Agilent ADS中文学习培训课程套装

ADS中文学习培训课程套装是迄今为止国内最全面最权威的ADS培训教程，详细全面地讲解了ADS在微波射频电路、通信系统和电磁仿真设计方面的内容。套装中的中文视频培训课程是由具有多年ADS使用经验的微波射频和通信领域资深专家讲解，工程实践强，且视频演示直观易学，能让您在最短的时间内学会使用ADS，并把ADS真正应用到微波射频电路和通信系统设计研发工作中去...。详情请浏览网址：http://www.mweda.com/eda/agilent.html

矢量网络分析仪学习套装

矢量网络分析仪是微波射频工程师研发调试工作中常用的测试仪器之一，为了帮助微波射频工程师最迅速、全面地熟悉掌握矢量网络分析仪使用，微波EDA网推出了这套矢量网络分析仪学习培训教程套装。套装中既有直观易学的矢量网络分析仪使用操作视频教程，也有全面的矢网用户操作手册，详情请浏览网址：http://www.mweda.com/vna/course

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台湾中华大学教授给岛内知名电子企业员工培训课程视频，由于是给企业员工培训，所以讲课内容尽量摒弃繁琐的数学推导、抽象的概念，多从工程实践出发，以通俗易懂的语言和直观工程实例来向学员讲述微波射频电路和数字通信系统相关知识。是从事微波射频电路设计和通信系统设计相关工程技术人员不可多得的经典学习教程。详情请浏览网址：http://www.mweda.com/vedio/vedio_45.html

Cadence Allegeo PCB设计培训套装

衡量一个软件的优劣，其中一个很现实的标准就是看它的市场占有率，Cadence Allegro现在几乎成为高速板设计中实际上的工业标准，被很多大型电子通信类公司采用，因此掌握Cadence Allegro对找份好工作有实质的帮助；另外其学习资源也比较丰富，比较适合自学。本站现推出Cadence Allegro PCB设计培训套装，实用易学，物超所值,帮助您迅速有效的学习掌握Allegeo PCB设计。详情请浏览网址：http://www.mweda.com/eda/allegro.html

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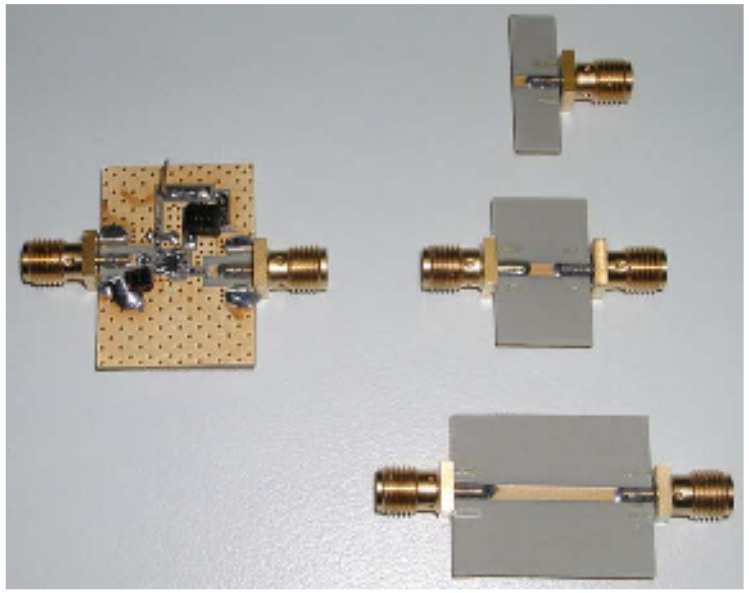
Practical RF Amplifier Design Using the Available Gain Procedure And the Advanced Design System EM/Circuit Co-Simulation Capability



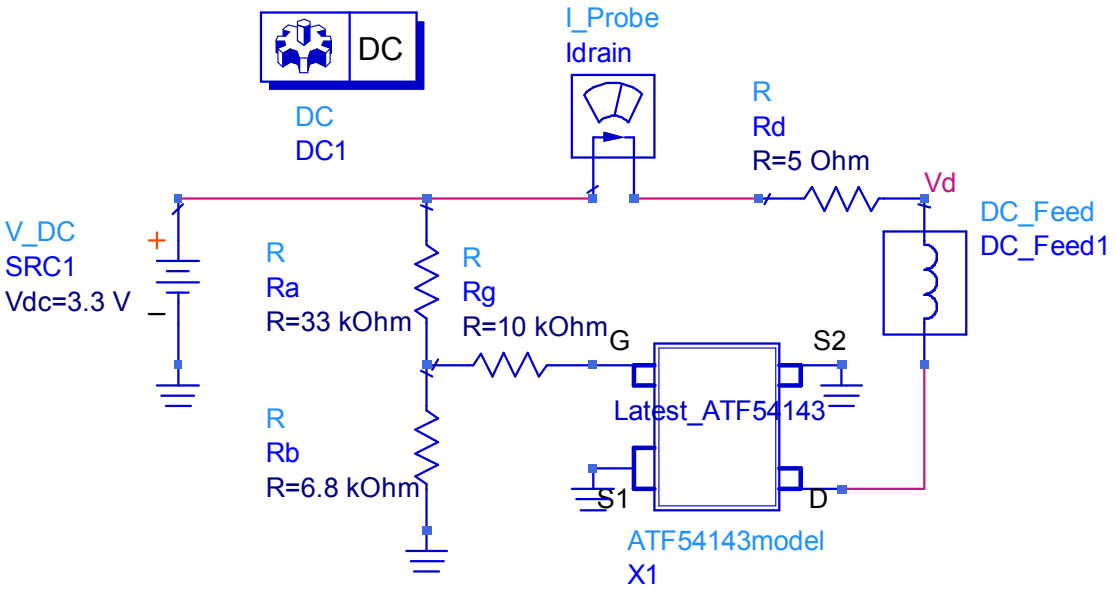
Introduction

- ✓ Focus on design flow rather than in-depth simulation setup overview.
- ✓ Vendor Supplied Design Information Importance (S-Parameters and Nonlinear Model)
- ✓ Use of ADS Momentum/Circuit Co-Simulation
- ✓ Use of ADS Design Guides to Speed Design Process
- ✓ Measured Versus Modeled
- ✓ Goal: One-Pass Design Process

802.11b Amplifier Design Requirements

- Frequency Range: 2.4GHz to 2.48GHz
- Gain: >12dB
- Noise Figure: <2.5dB
- Input Return Loss: >10dB
- Output Return Loss: >10dB
- Third Order Input Intercept Point: >0dBm
- Supply Current: <100mA

Nonlinear Model Bias and DC Simulation

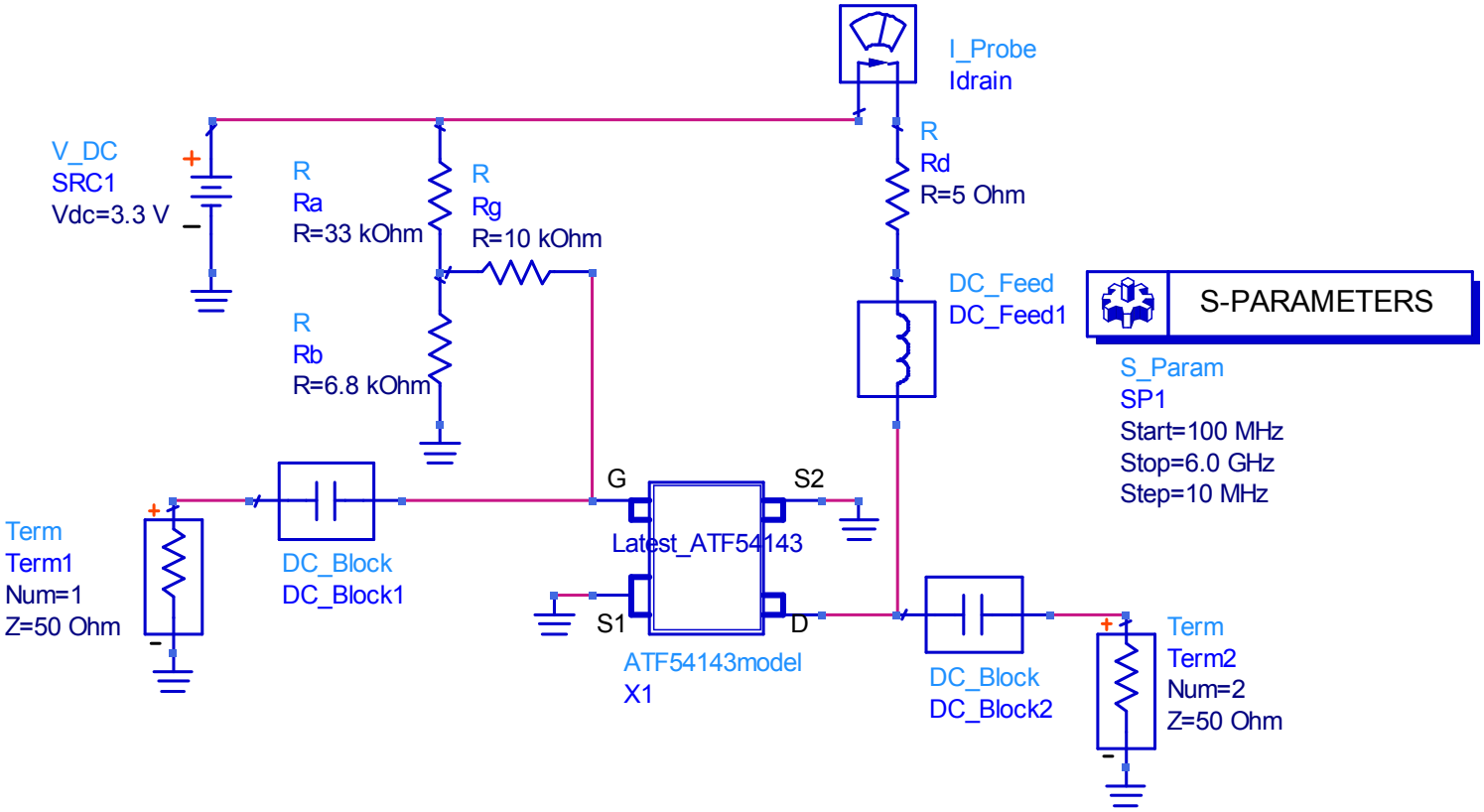


freq	Idrain.i	Vd
0.0000 Hz	61.38 mA	2.993 V

- The Avago ATF54143 has measured s-parameter and noise parameter data at various bias conditions including a 3.0V V_{DS} and 60mA I_{DS}. The nonlinear model is biased at the same DC operating point as was the device for the measured s-parameter data provided by Avago. The ATF54143 is an enhancement mode FET that requires a positive gate voltage with respect to its source to obtain the desired drain-to-source bias current of 60mA.

- A voltage divider network is provided by Ra and Rb and is adjusted in the simulator to quickly obtain the required 60mA drain-to-source current.

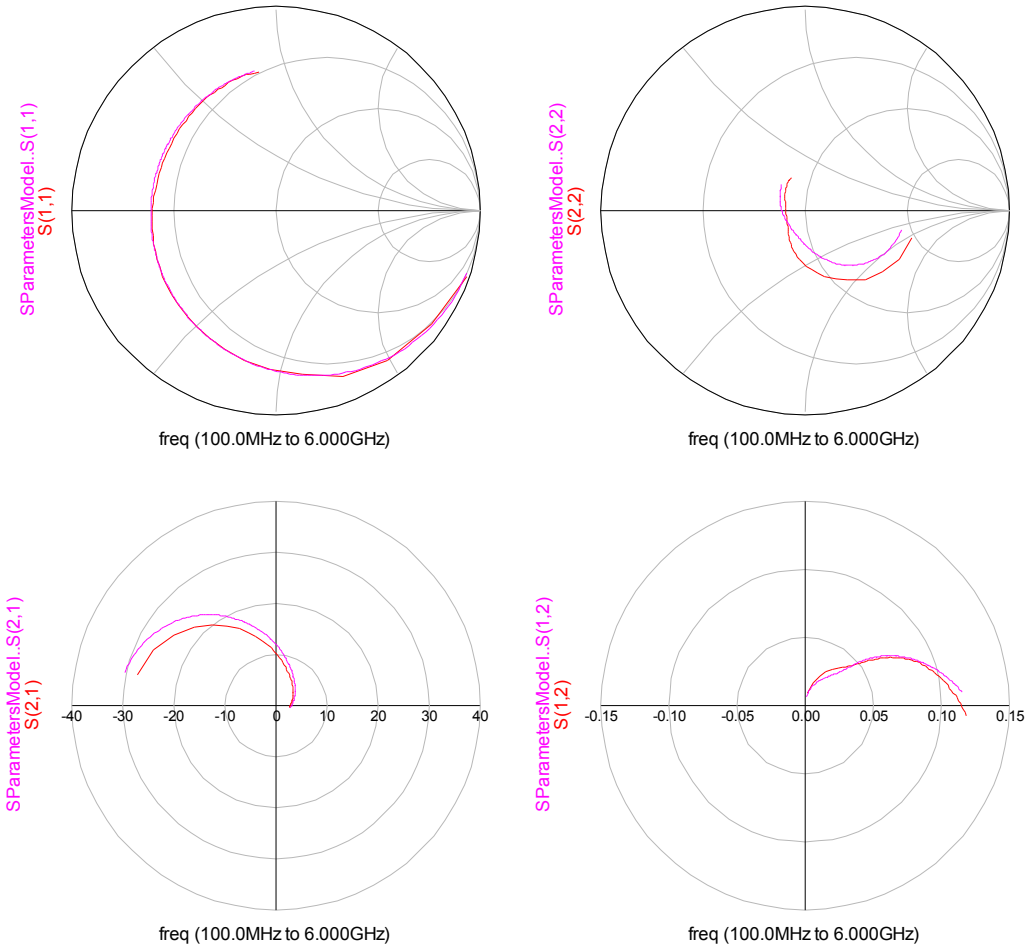
Nonlinear Model Generated S-Parameter Data



• DC blocking capacitors and 50Ω terminations are added to the DC biased nonlinear circuit input and output to obtain nonlinear model generated S-parameters from 100MHz to 6GHz with a frequency step of 10MHz.

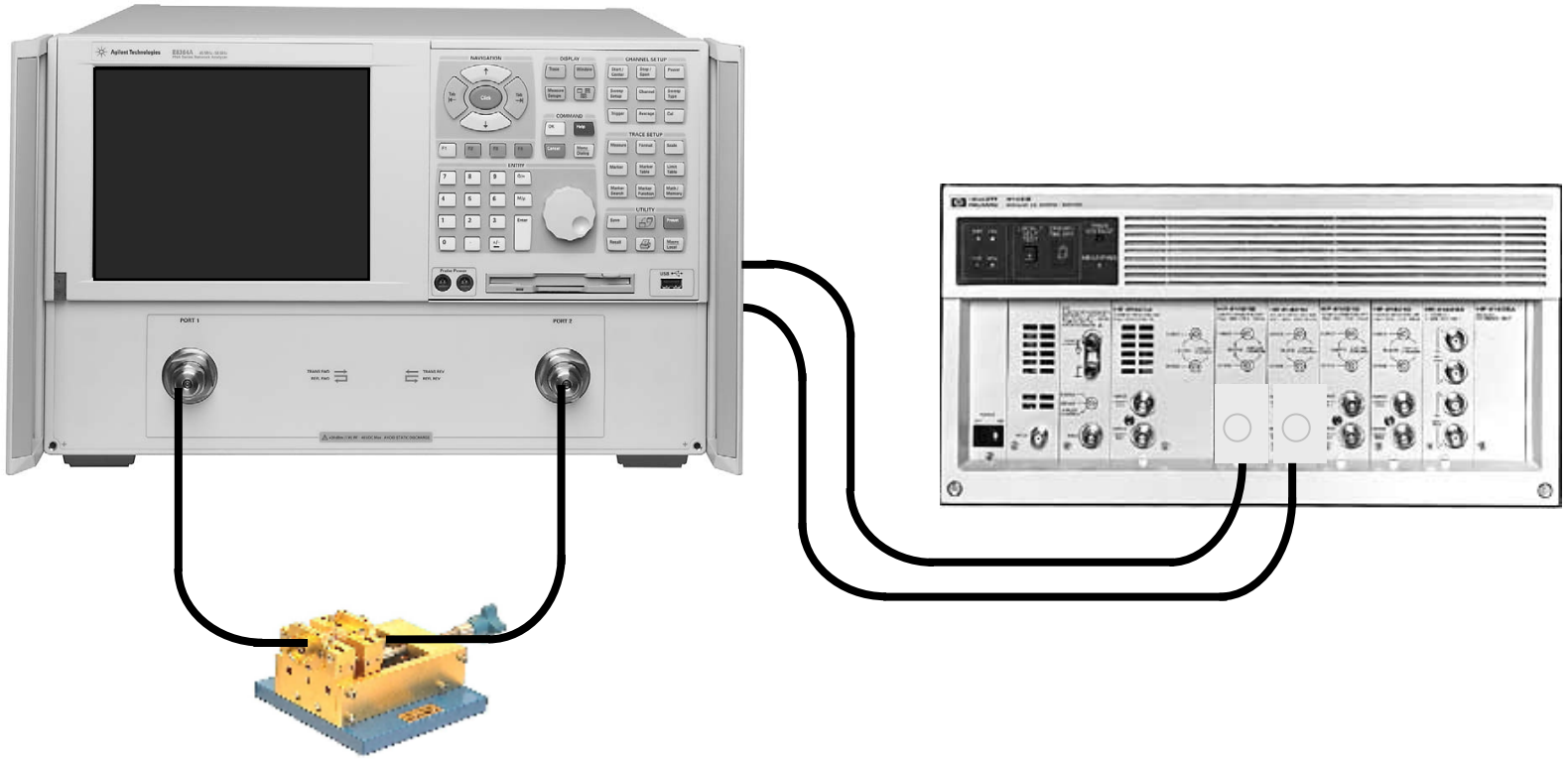
• S-parameter data is obtained from 100MHz to 6GHz with a frequency step of 10MHz.

Nonlinear Model Versus Measured S-Parameters



Nonlinear model generated s-parameters and the Avago measured s-parameter data closely match.

S-Parameter Data Validation

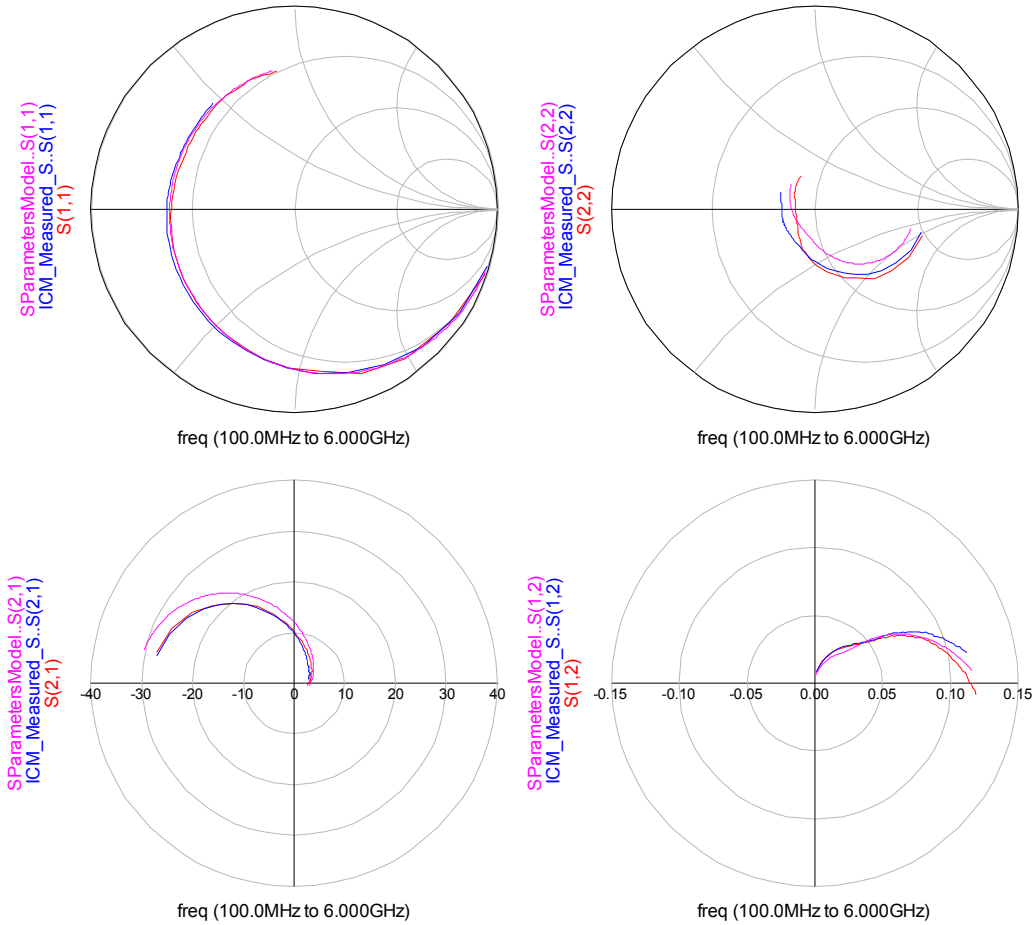


• An Intercontinental Microwave transistor test fixture with the appropriate midsection is used to measure transistor S-parameters.

• Before calibration is performed, all TOSL-3001 calibration coefficients are loaded into the network analyzer. Limit network analyzer source power to –25dBm.

• The HP4142B DC Source/Monitor is connected to the E8364B network analyzer bias tees located on the back of that instrument to bias the transistor at 3.0V V_{DS} and 60mA I_{DS}.

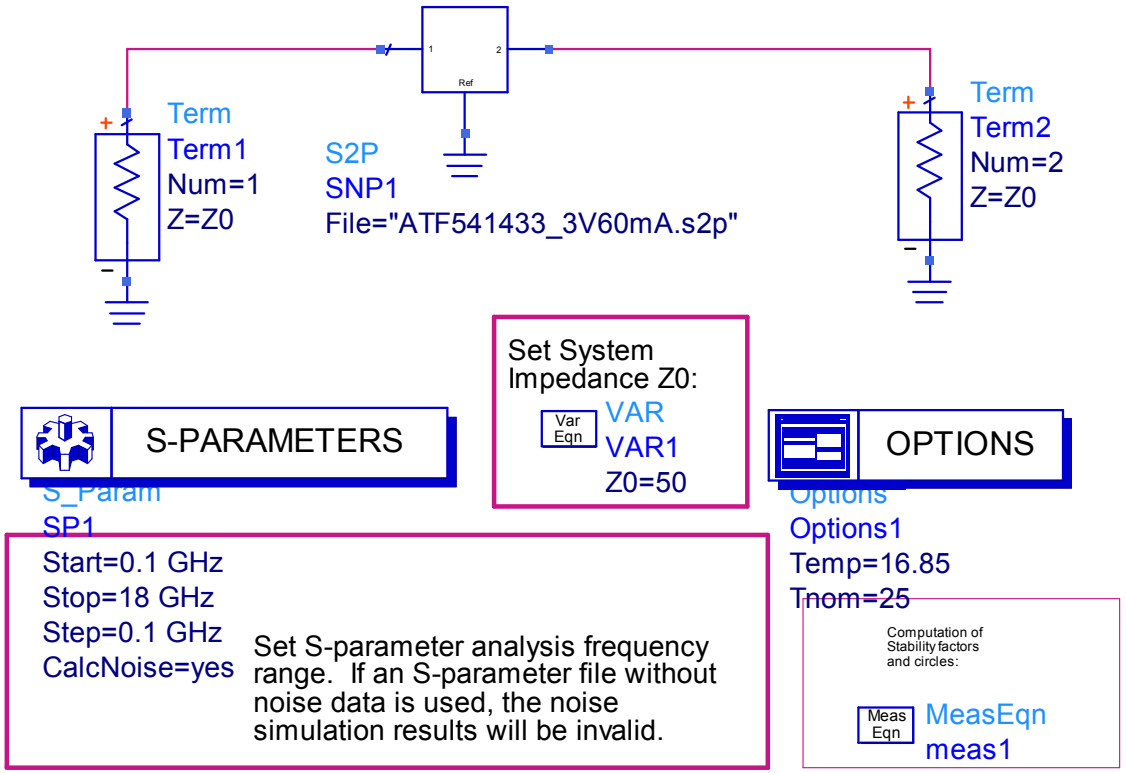
Lab Measured Versus Avago S-Parameters



Avago measured s-parameters, nonlinear model generated s-parameters, and the lab measured s-parameters are in close agreement with each other.

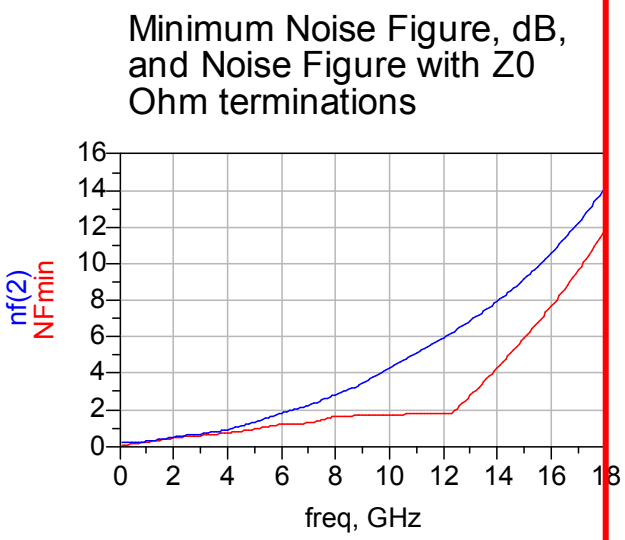
ATF54143 Transistor Stability Analysis

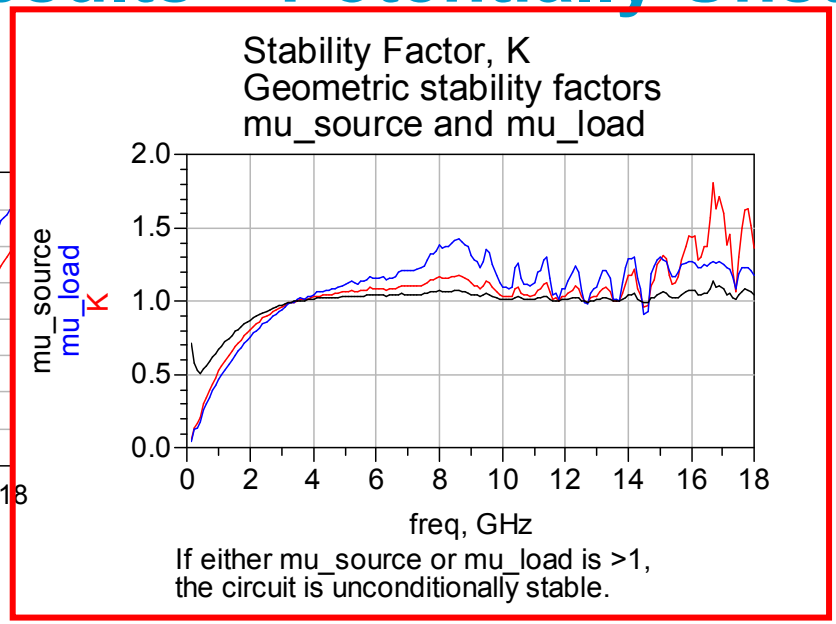
S-Parameters, Noise Figure, Gain, Stability, Circles, and Group Delay versus Frequency



- It is highly recommended that the amplifier circuit is made unconditionally stable at all frequencies to ensure that it does not produce unwanted oscillations.
- An ADS Amplifier Design Guide quickly calculates and displays circuit stability.

Transistor Stability Results – Potentially Unstable

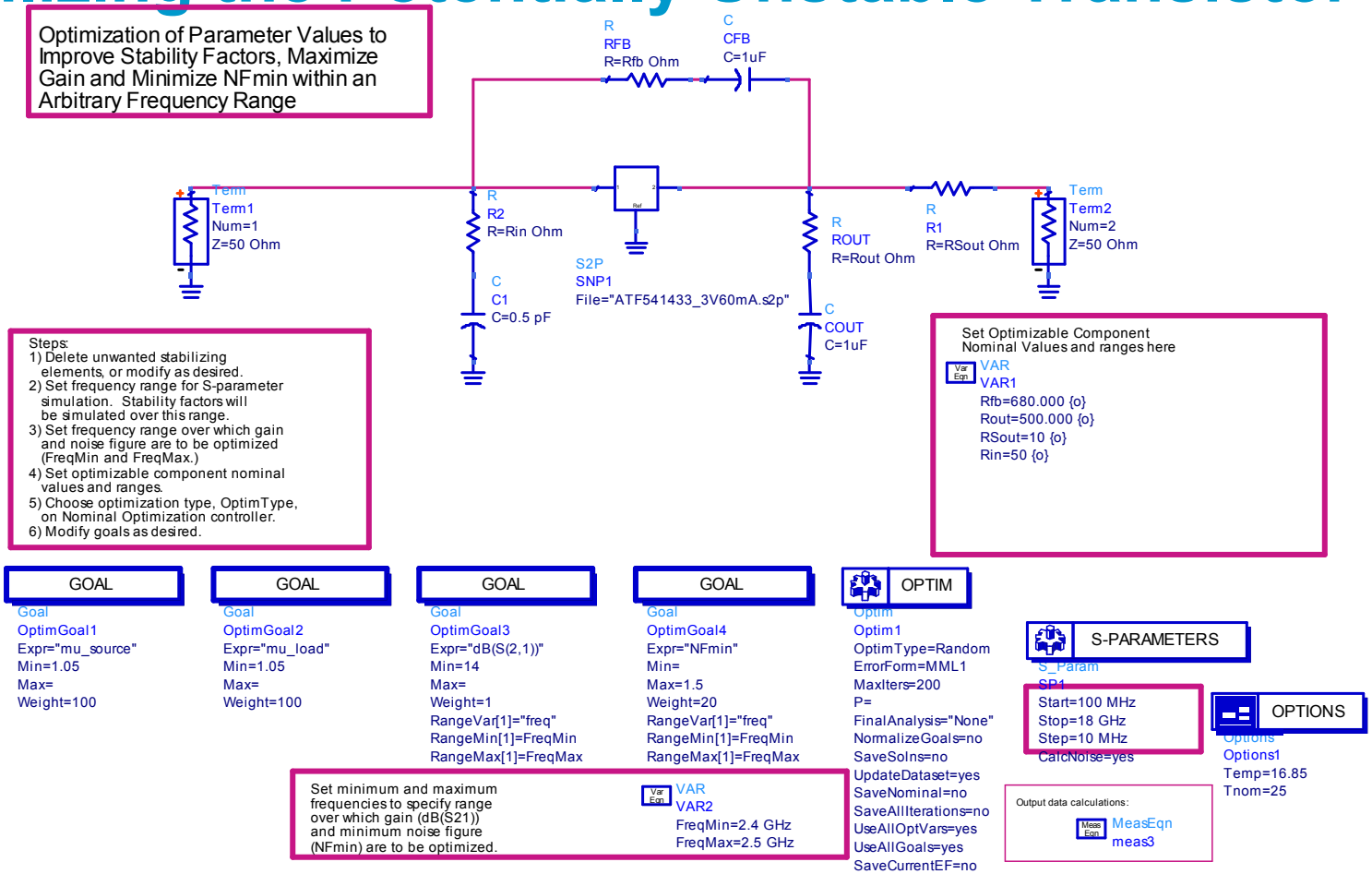




- To achieve unconditional stability, the circuit must have $K \geq 1$ and {$|\Delta| < 1$ or $B1 > 0$ or $B2 > 0$}; or separately geometric stability factors $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$.
- Observation of the Stability Factor K, geometric stability factors μ_{source} and μ_{load} indicate potential instability below 4GHz and marginal unconditional stability above 4GHz.
- One way to ensure stability as far as environmental conditions are concerned is to provide significant margin to the stability conditions. In other words, make $K >> 1$ at all frequencies.
- It is important to stabilize this device and obtain unconditional stability at all frequencies.

Stabilizing the Potentially Unstable Transistor

Optimization of Parameter Values to Improve Stability Factors, Maximize Gain and Minimize NFmin within an Arbitrary Frequency Range



• Transistors are stabilized through the use of series and parallel feedback and series and parallel loading at the input and output. A combination of these networks may be necessary to get the desired stability results. Since this amplifier is used in a low noise application, it is desirable to limit loss at the device input at the operating frequency, which degrades amplifier noise figure.

Stabilizing the Potentially Unstable Transistor

• Capacitor CIN is changed to 0.5pF to limit input loading at the operating frequency since loss added at the input degrades noise figure. The 0.5pF capacitor has a relatively high reactance at 2.5GHz and this reactance decreases with an increase in frequency. This allows input parallel loading at higher frequencies and very little loading at 2.5GHz.

• The resistive feedback helps stabilize the circuit at low frequencies and has little impact at the operating frequency.

• The optimization goals are set to optimize for stability, maximum gain, and minimum noise figure.

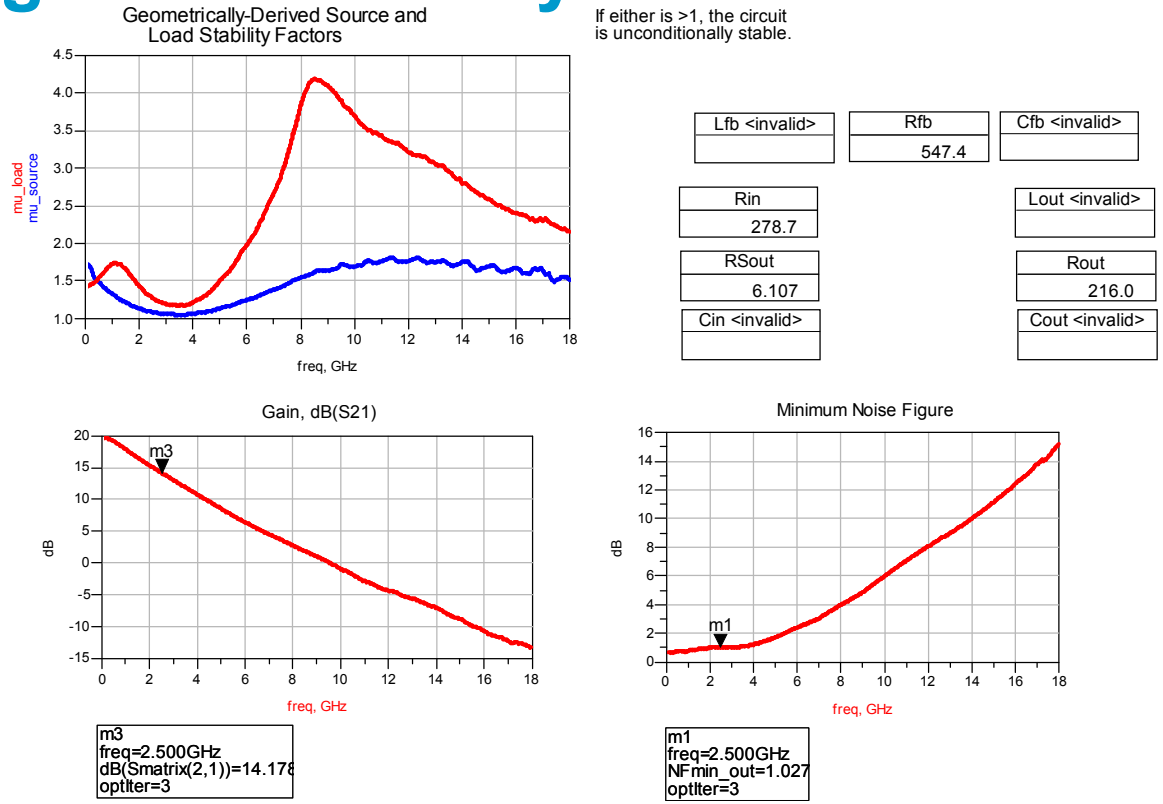
• Stability goals OptimGoal1 and OptimGoal2 are set to a Min=1.05 as a default over the entire simulation frequency range. These goals ensure that $\mu_{source} \geq 1$ and $\mu_{load} \geq 1$, which indicates unconditional stability.

• OptimGoal3 is set to a Min=14dB for dB(S21) over the 2.4GHz to 2.5GHz operating frequency range.

• The noise figure goal is set to a Max=1.5dB from 2.4GHz to 2.5GHz.

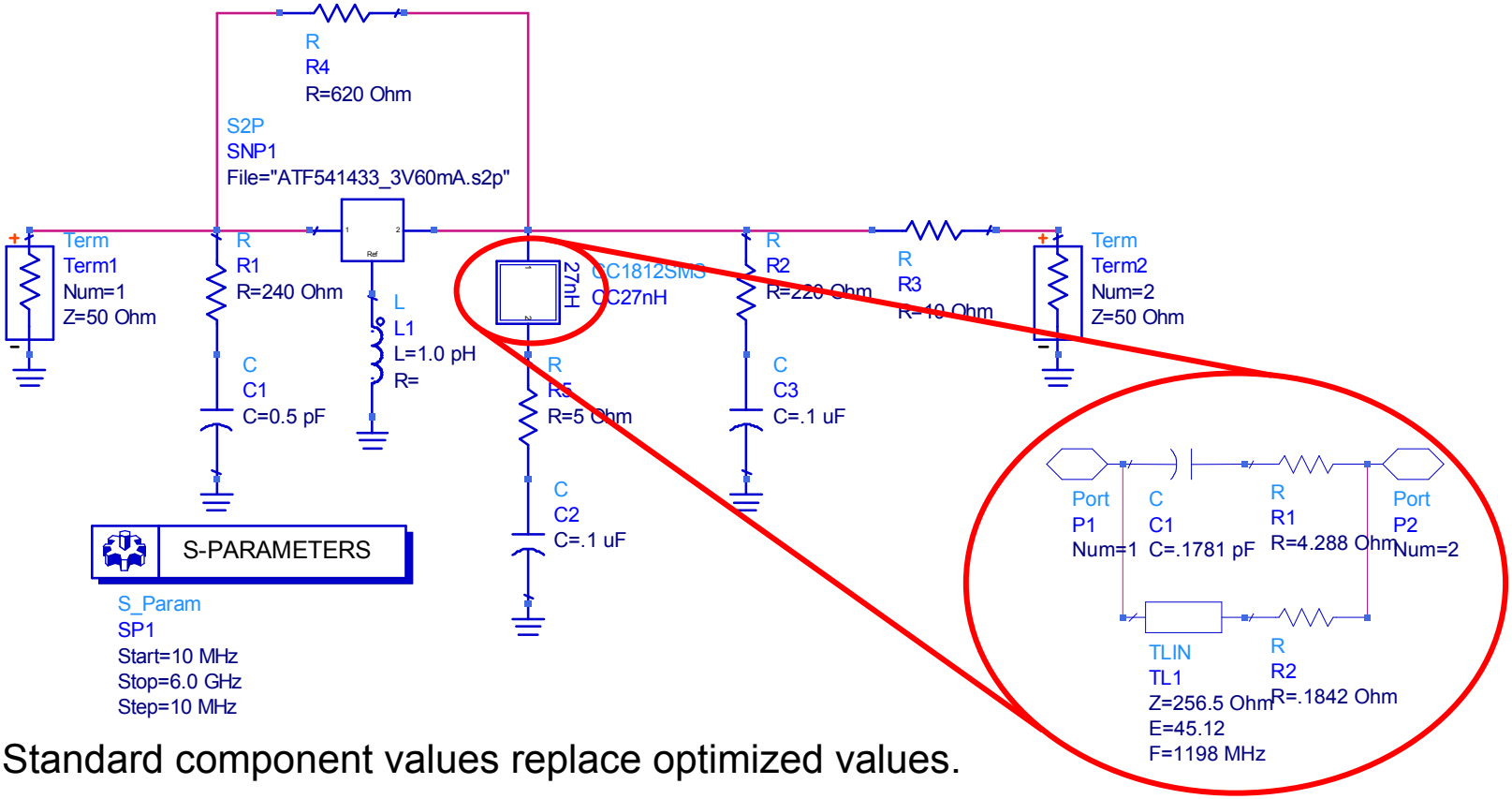
• Optimized component values: Rfb=547Ω, Rin=279Ω, RSout=6Ω, Rout=216Ω.

Stabilizing the Potentially Unstable Transistor



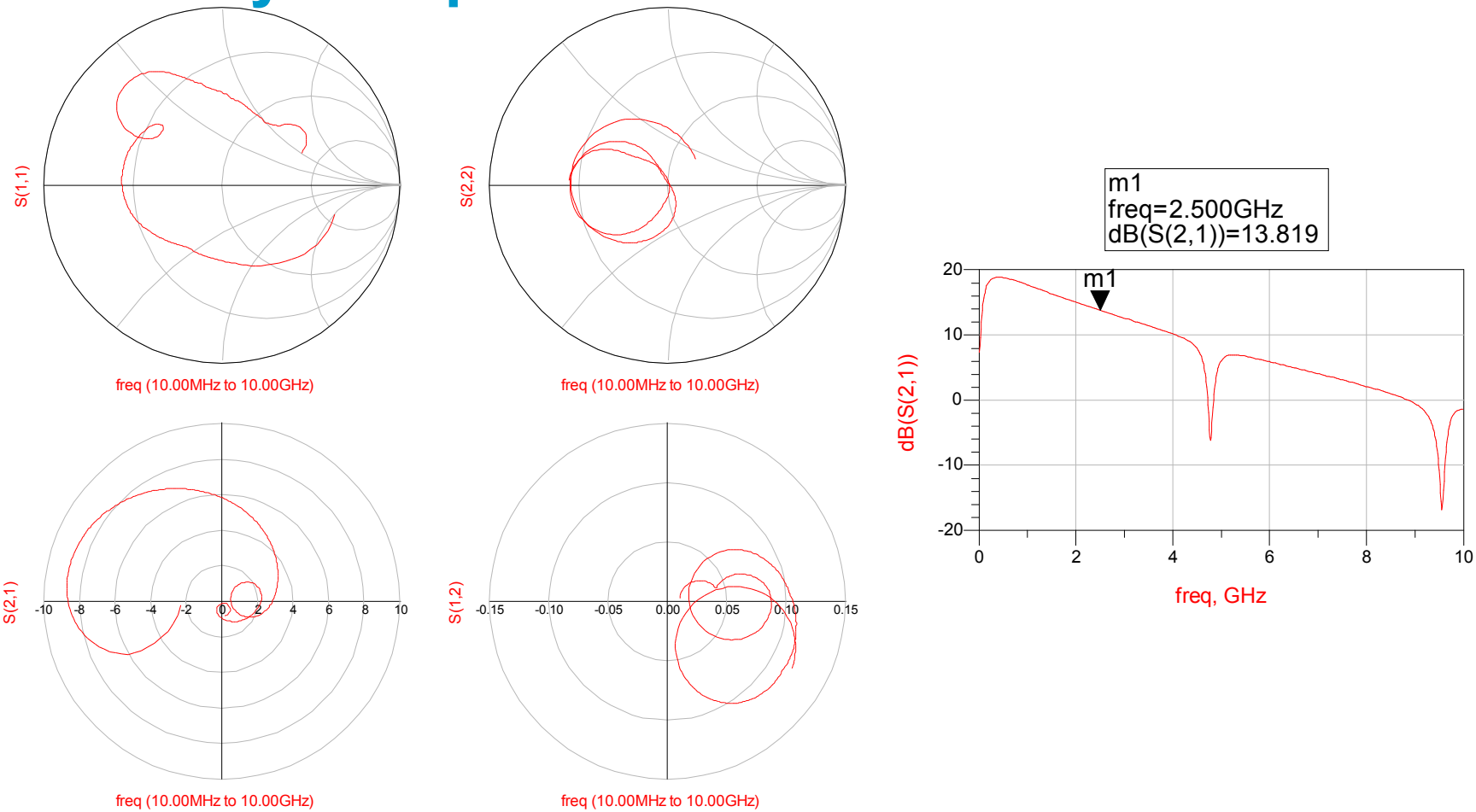
- Observation of geometric stability factors μ_{source} and μ_{load} indicates unconditional stability at all frequencies since $\mu_{source} \geq 1$ or $\mu_{load} \geq 1$.
- Preliminary optimized circuit performance: Gain=14.2dB, Minimum Noise Figure=1dB.
- Typically, if the preliminary analysis does not meet the design criteria, then the final circuit with parasitics doesn't meet the objectives. In other words, parasitics typically degrade RF performance.

Preliminary Component and PCB Parasitics



- Standard component values replace optimized values.
- Component parasitics include loss and unexpected reactance.
- An equivalent circuit model of a Coilcraft Midi series air-wound inductor replaces the ideal DC feed. Ideally, a very large inductance is needed for the DC feed coil. Inductor parasitic capacitance limits the allowable inductance value due to self-resonance. A Coilcraft Midi Series 27nH inductor has a 2.7GHz minimum self-resonant frequency.

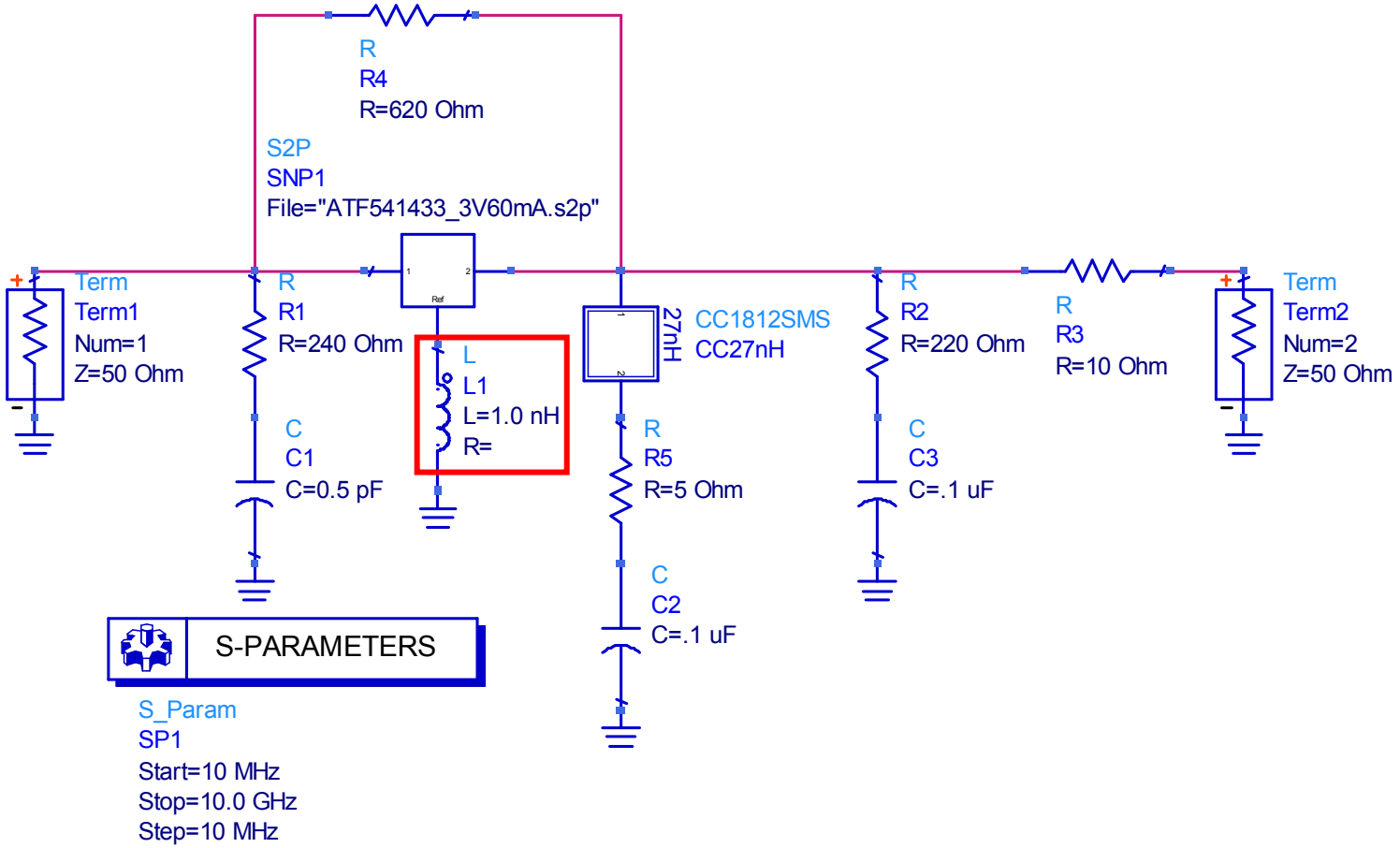
Preliminary Component and PCB Parasitics



• Both |S11| and |S22| are inside the unit radius Smith chart, which is a necessary, but not sufficient condition for unconditional stability.

• The 50Ω gain of 13.82dB is slightly lower than the original 14.17dB because of resistors changed to standard values and the additional loss added by the inductor.

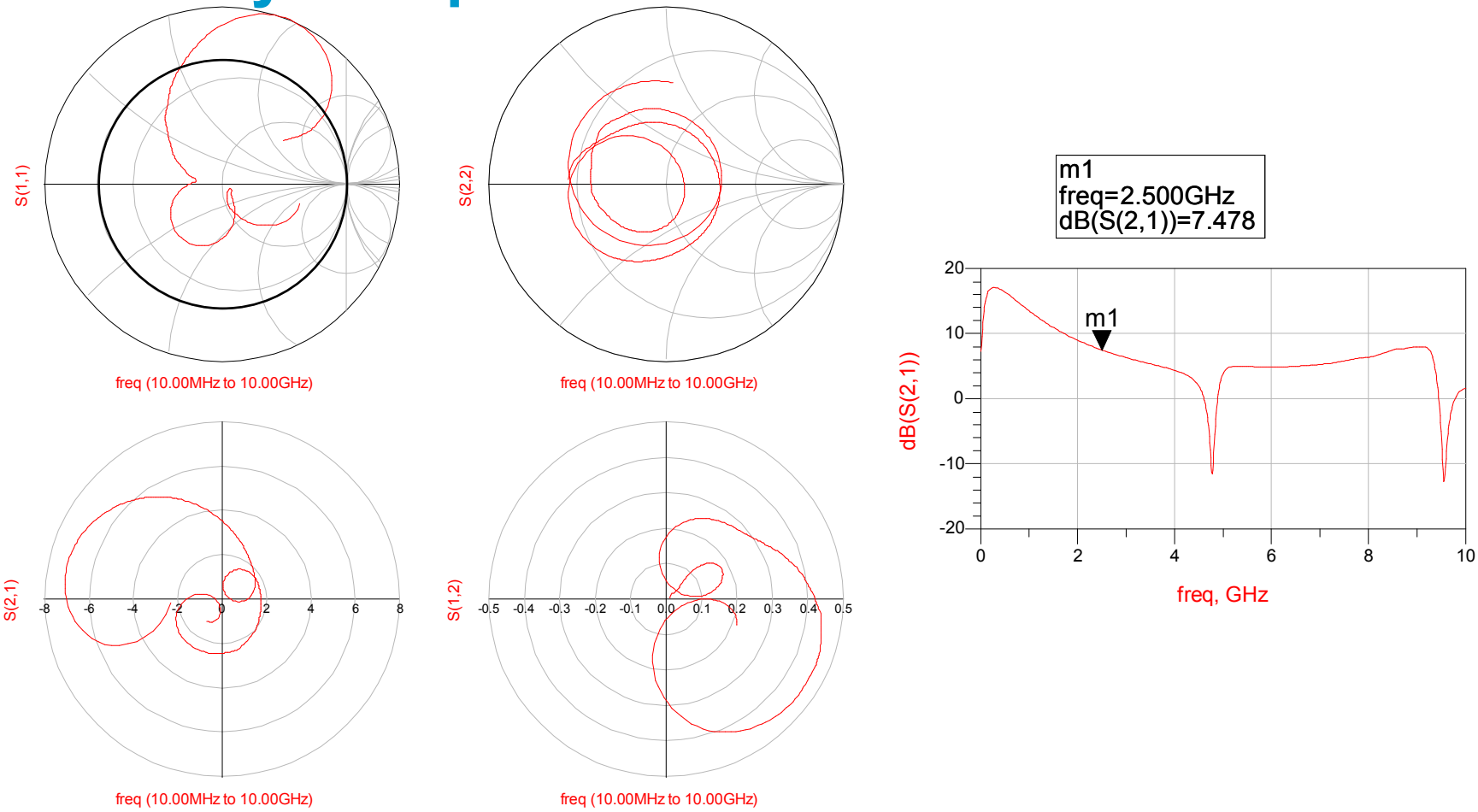
Preliminary Component and PCB Parasitics



• An arbitrary value of 1nH in the transistor source ground return path is used to get an indication on how sensitive the circuit is to parasitic ground inductance.

• Higher values of transistor source or emitter lead ground inductance are not uncommon in PCB layouts.

Preliminary Component and PCB Parasitics



• The |S11| is outside the unit radius Smith chart indicating an input reflection coefficient magnitude greater than unity. Small amounts of parasitic ground inductance make this circuit potentially unstable at some frequencies.

• The dB(S21) plot shows the 50Ω gain at 2.5GHz is reduced from 13.82dB to 7.48dB.

Preliminary Component and PCB Parasitics

• Layout parasitics that can wreak havoc on RF circuit performance include ground or lead inductance and parasitic capacitance on the signal path. Minute amounts of ground or lead inductance can cause a calculated unconditionally stable circuit to become unstable.

• Layout for this circuit is critical with respect to the parasitic ground inductance.

• Since the input reflection coefficient magnitude is greater than unity, a stability analysis is not necessary to determine whether or not the amplifier has a propensity to oscillate.

• Ground inductance causes circuit gain to be significantly less than gain predicted with ideal s-parameter simulations.

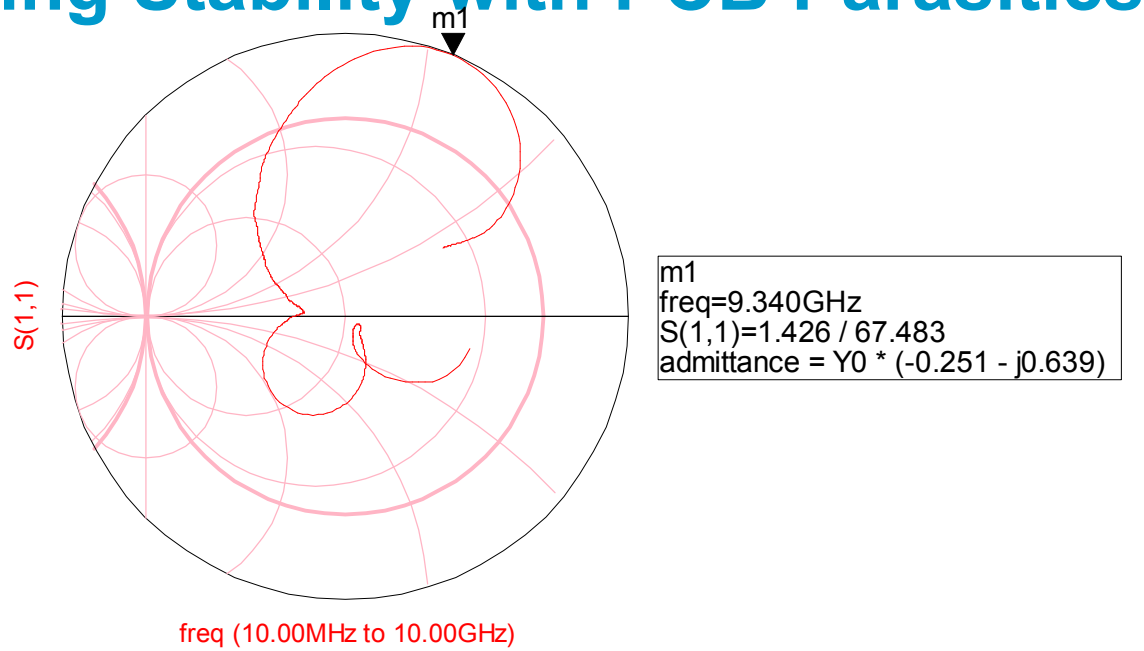
• The stability networks need to load the circuit more out-of-band in case the layout parasitic ground inductance is not low enough.

• There is no way to totally eliminate the ground inductance, thus, more loading may be required for stability margin.

• Since the transistor high input reflection coefficient is causing the problem, loading the output has little affect on stability for this circuit.

• Every effort is made to minimize layout ground inductance so the amplifier meets the gain requirement and does not oscillate.

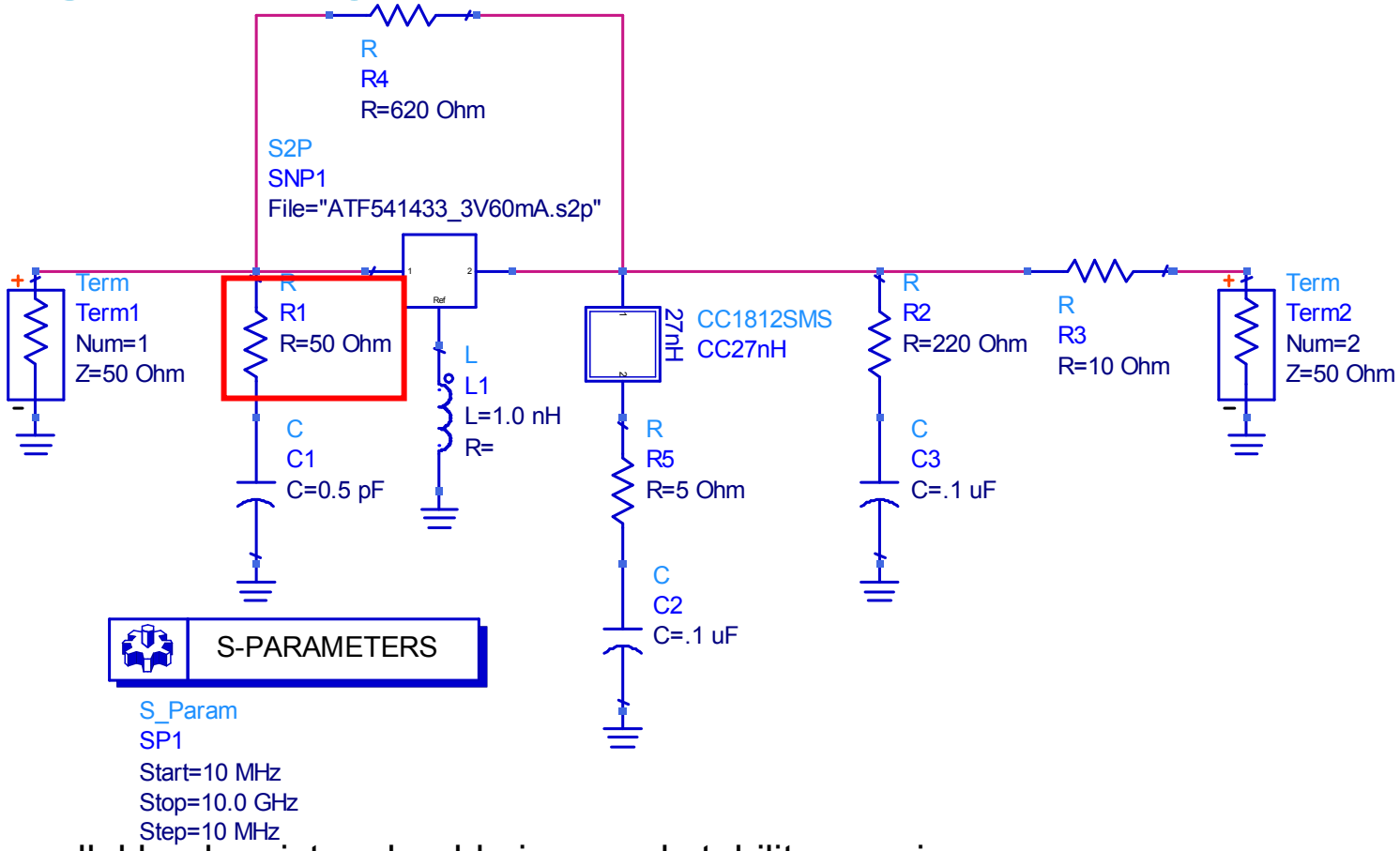
Ensuring Stability with PCB Parasitics



• The input reflection coefficient plotted on an admittance plane Smith chart. The marker is moved to a location on the trace that has the highest value of negative conductance. The reciprocal of the conductance gives the additional parallel load necessary to move the input reflection coefficient to the edge of the Smith chart. This provides little stability margin. Currently, the input is loaded with a parallel 240Ω resistor at high frequencies.

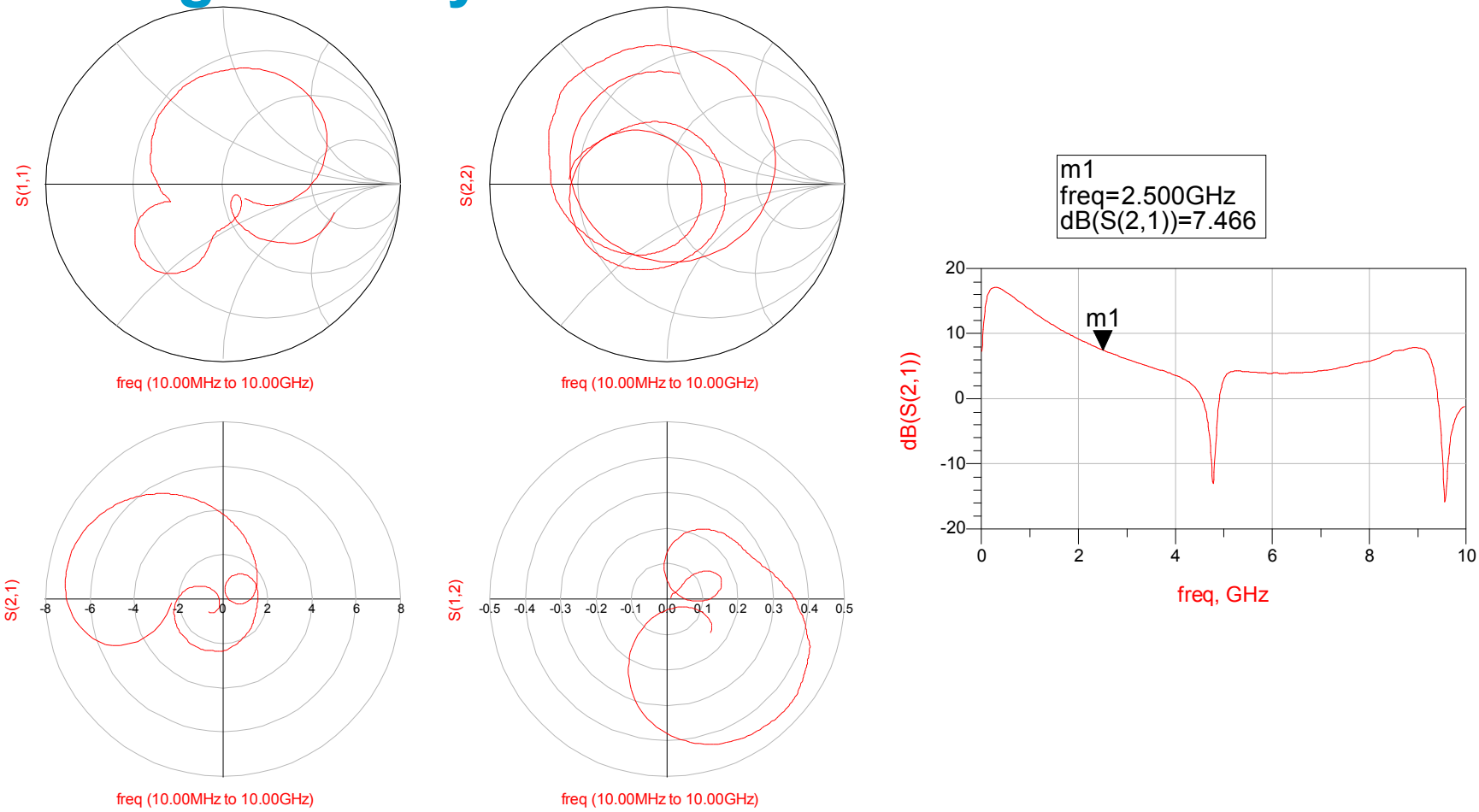
• An additional parallel input load of 200Ω moves the input reflection coefficient to the edge of the Smith chart. This gives a total required parallel resistance of 109Ω to move the input reflection coefficient to the Smith chart edge. This gives no stability margin.

Ensuring Stability with PCB Parasitics



- A 50Ω parallel load resistor should give good stability margin.
- The 50Ω gain is 7.47dB which is only 0.01dB less than the case with the 240Ω input parallel resistive load. This shows that the input loading has little affect on the circuit at 2.5GHz due to the 0.5pF capacitor being used as the bypass, but has a huge affect at higher frequencies

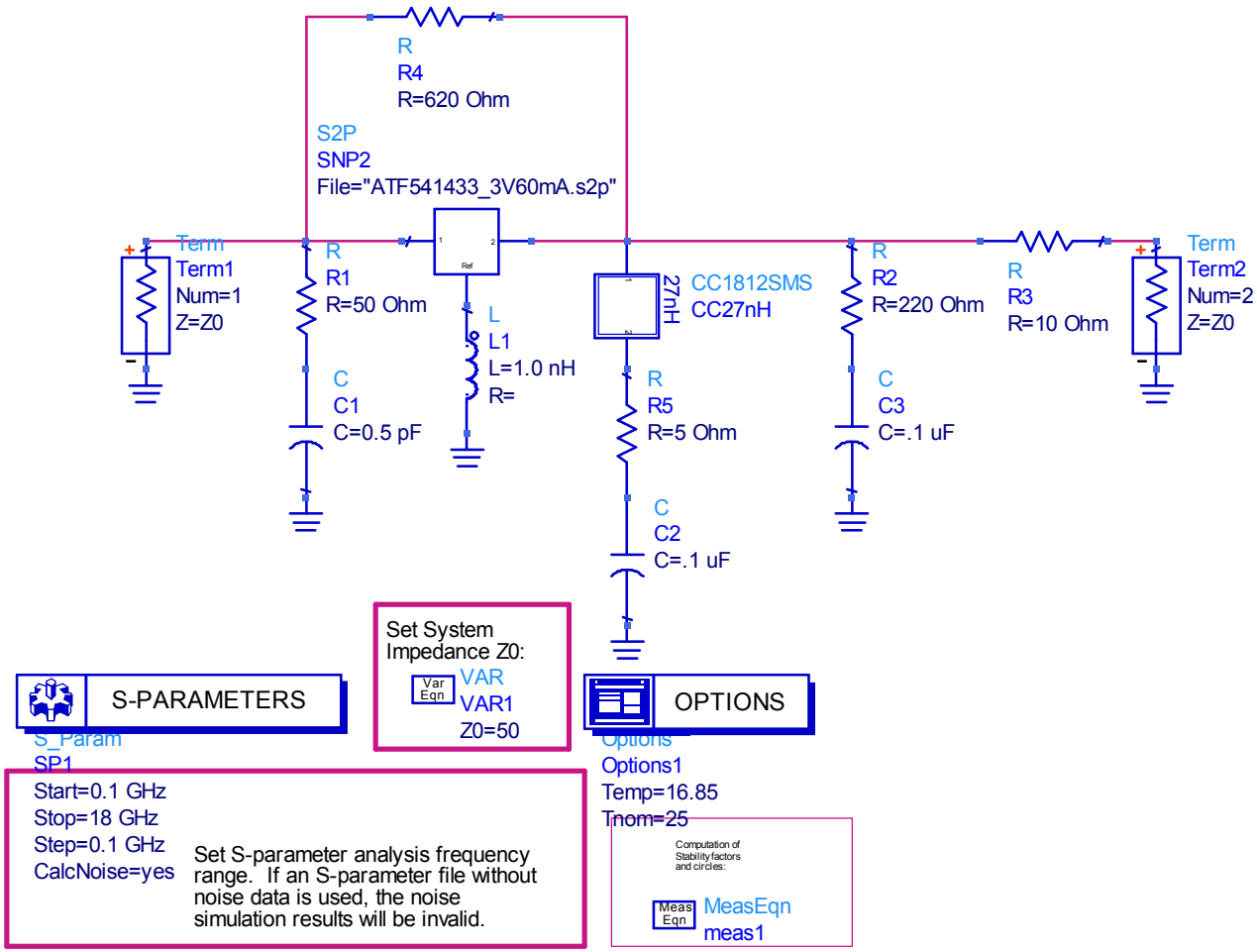
Ensuring Stability with PCB Parasitics



• Since both input and output reflection coefficient magnitudes remain less than unity when the circuit input and output is terminated with 50Ω, a stability analysis is now performed.

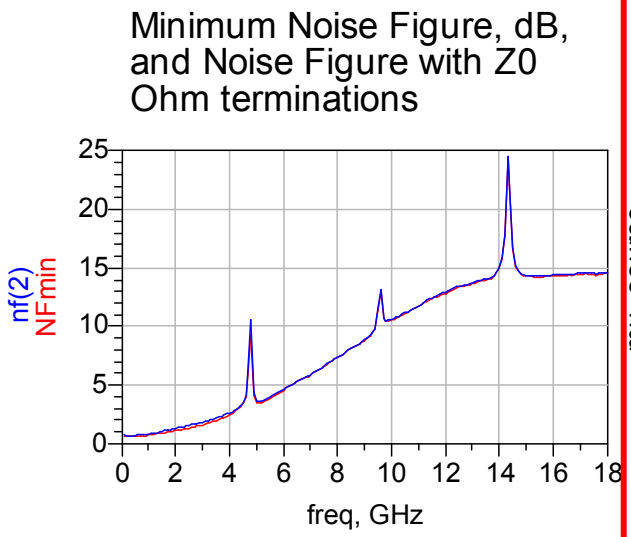
Ensuring Stability with PCB Parasitics

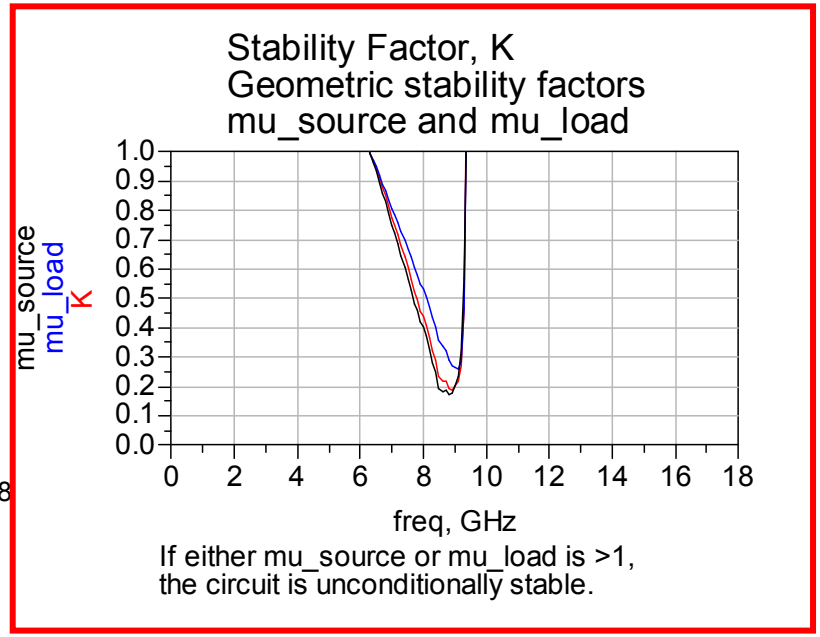
S-Parameters, Noise Figure, Gain, Stability, Circles, and Group Delay versus Frequency



- The stability analysis is set up using an ADS Amplifier Design Guide.

Ensuring Stability with PCB Parasitics



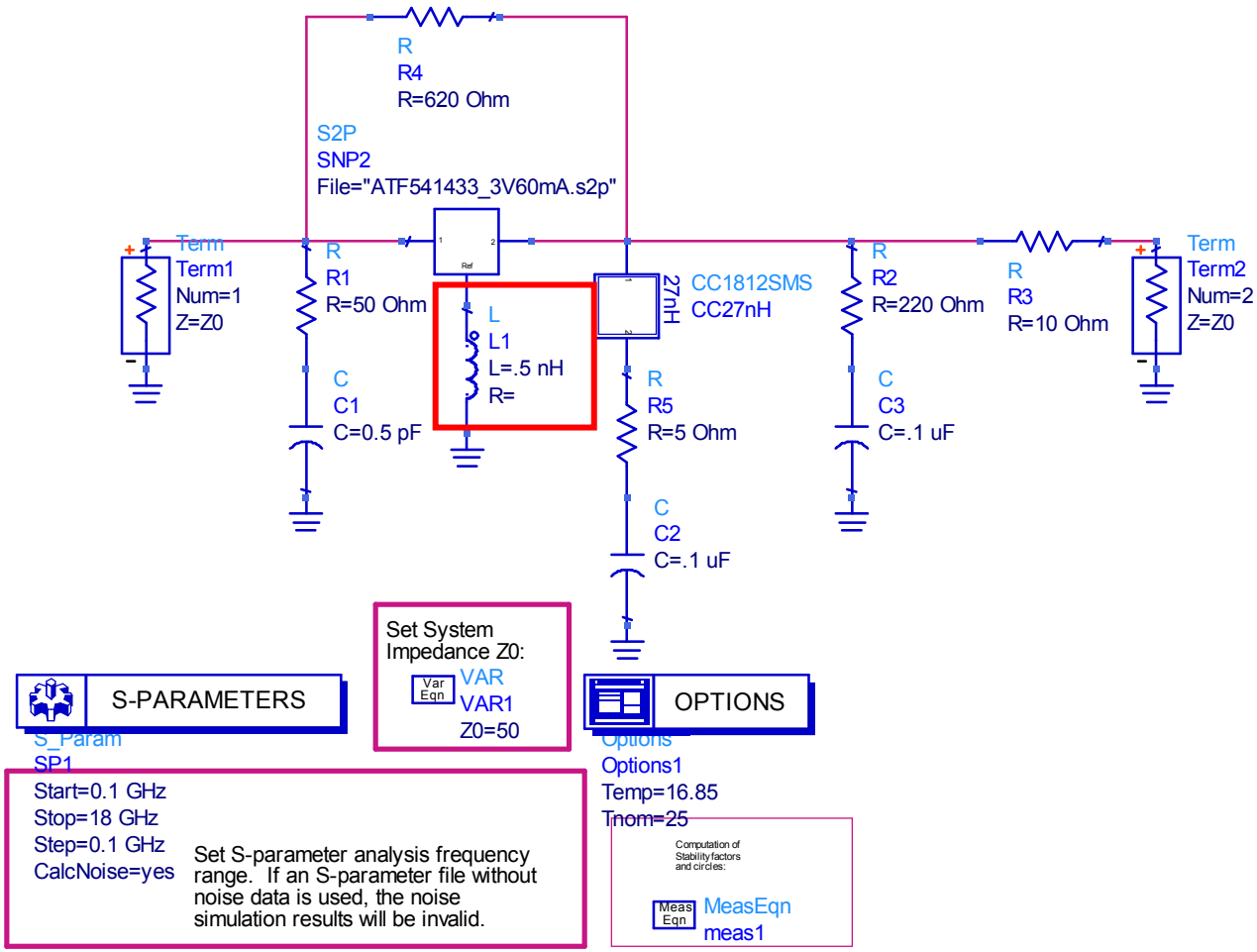


• The circuit indicates potential instability between 6GHz and 9.5GHz as shown in the red box since μ_{source} <1 and μ_{load} <1.

• Before making any further adjustments to stabilizing networks, the parasitic ground inductance is adjusted down to 0.5nH. The 1nH value was arbitrarily chosen to begin with, so it is helpful to see how sensitive the circuit is when the parasitic ground inductance is cut in half.

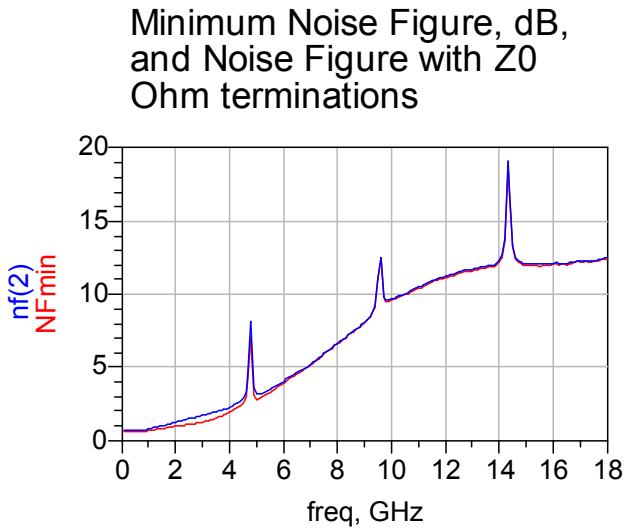
Ensuring Stability with PCB Parasitics

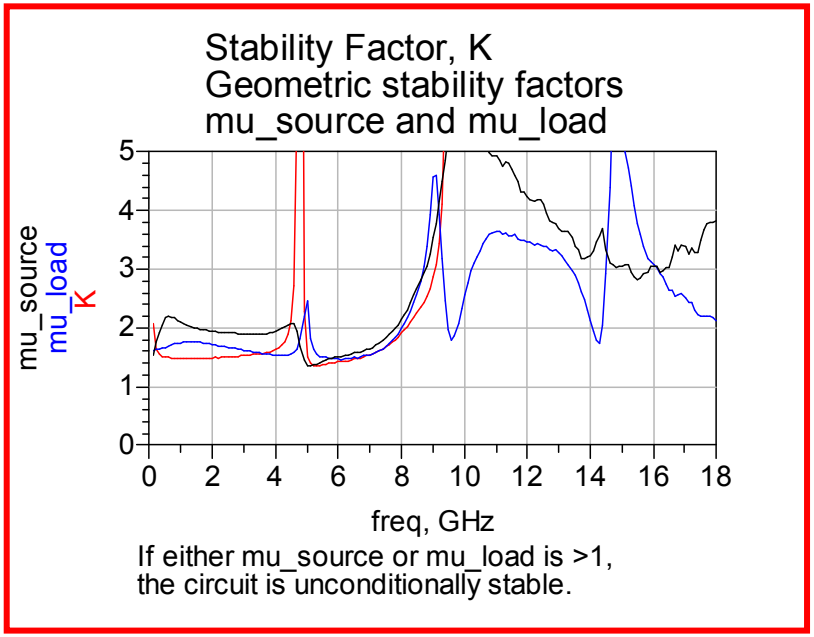
S-Parameters, Noise Figure, Gain, Stability, Circles, and Group Delay versus Frequency



The parasitic ground inductance is set to 0.5nH.

Ensuring Stability with PCB Parasitics



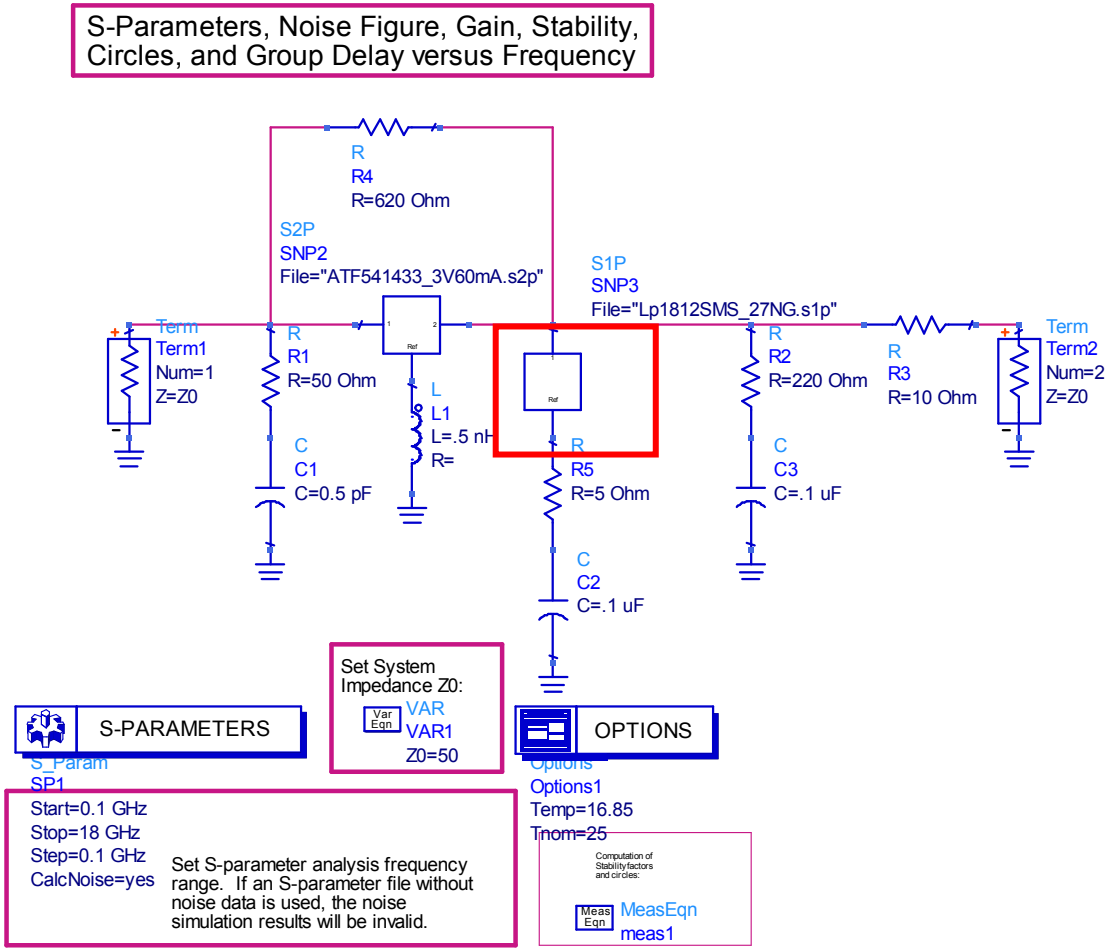


• K, μ_{source}, and μ_{load} are plotted and indicate unconditional stability from 100MHz to 18GHz with more stability margin at higher frequencies as desired.

• At this stage of the design, it is not yet known how much parasitic ground inductance is contained in the PCB layout. Special attention is given to the layout procedure to ensure that parasitic ground inductance is kept as low as possible.

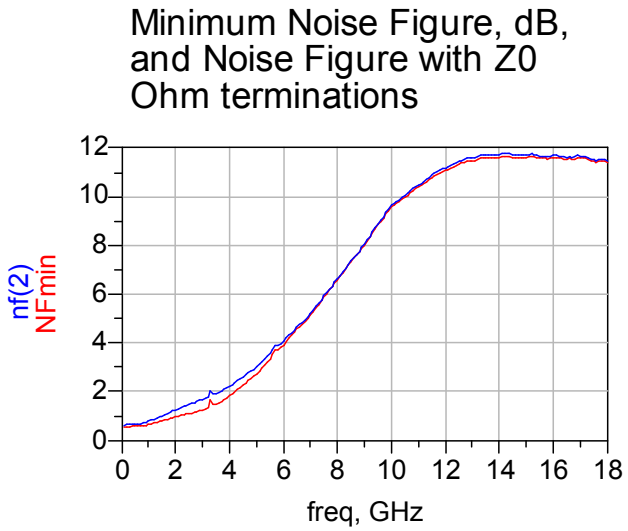
• The stability plots show three spikes over the 100MHz to 18GHz frequency range. The transmission line used in the Coilcraft 27nH inductor model causes these spikes. The actual Coilcraft inductor does not behave as suggested by the model above its self-resonance frequency.

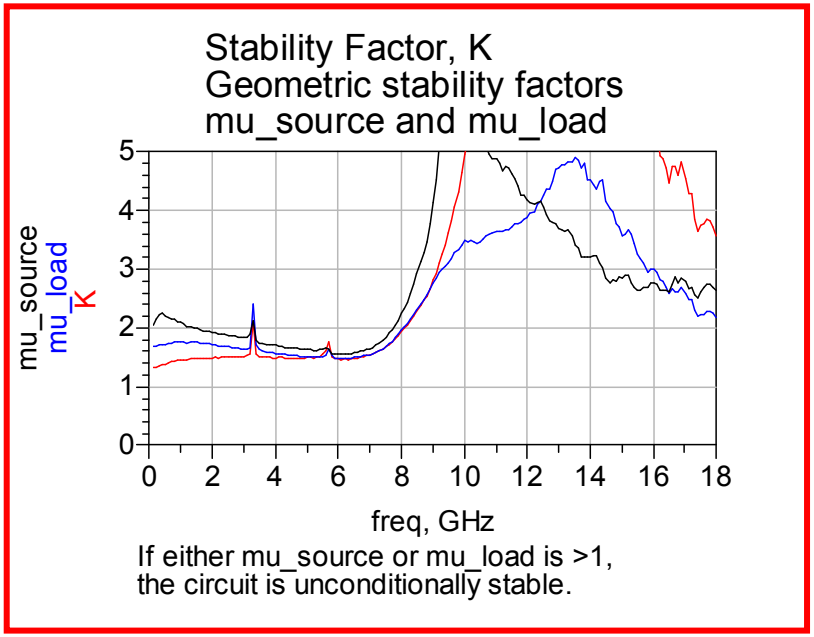
Ensuring Stability with PCB Parasitics



• A one-port measurement of the inductor is saved to a touchstone file named Lp1812SMS_27NG. This one-port measured data file is now used in the simulation to more accurately predict the behavior above the self-resonant frequency of the inductor up to 6GHz and eliminate the “data spikes”.

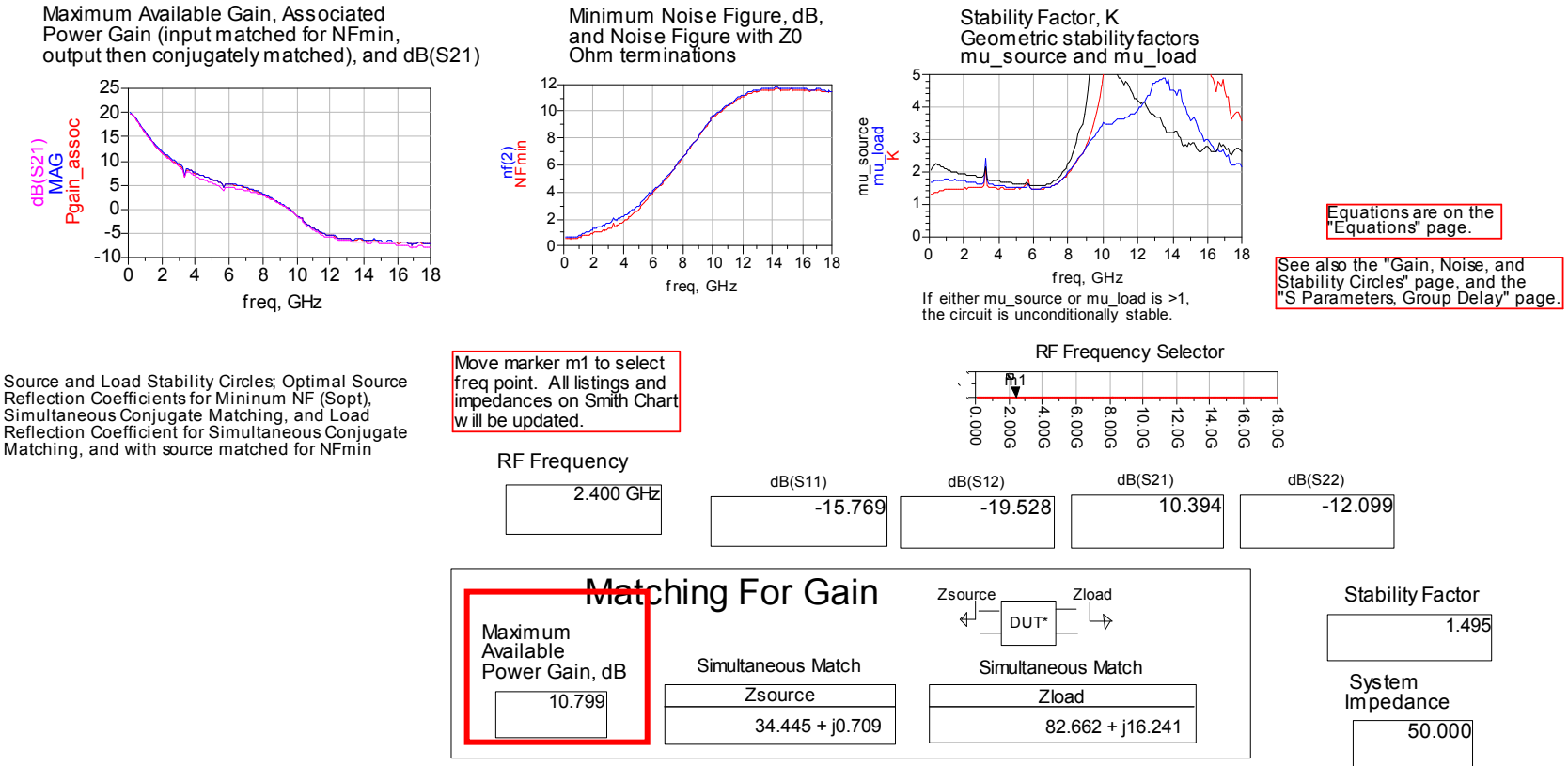
Ensuring Stability with PCB Parasitics





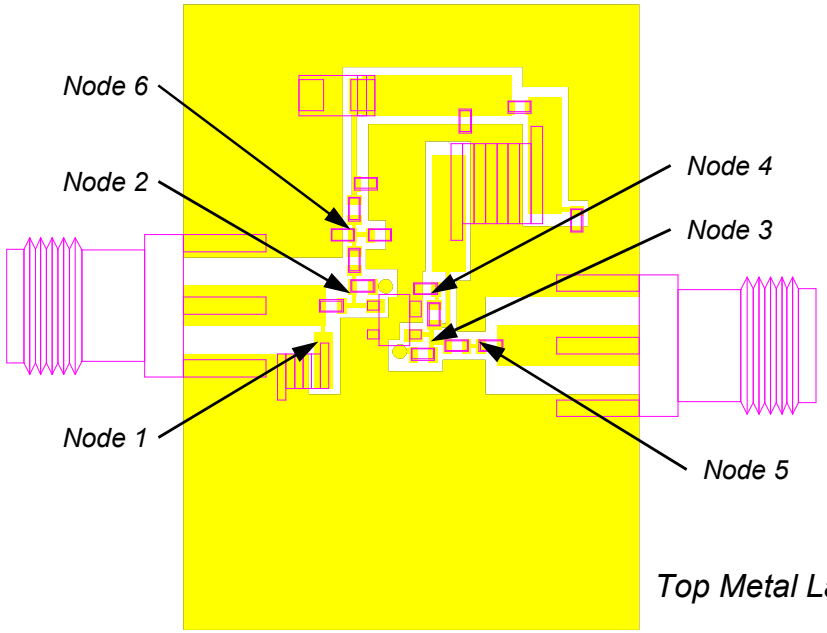
The inductor primary self-resonant frequency response is still noticeable in the amplifier frequency response plots as expected, although it is not as pronounced.

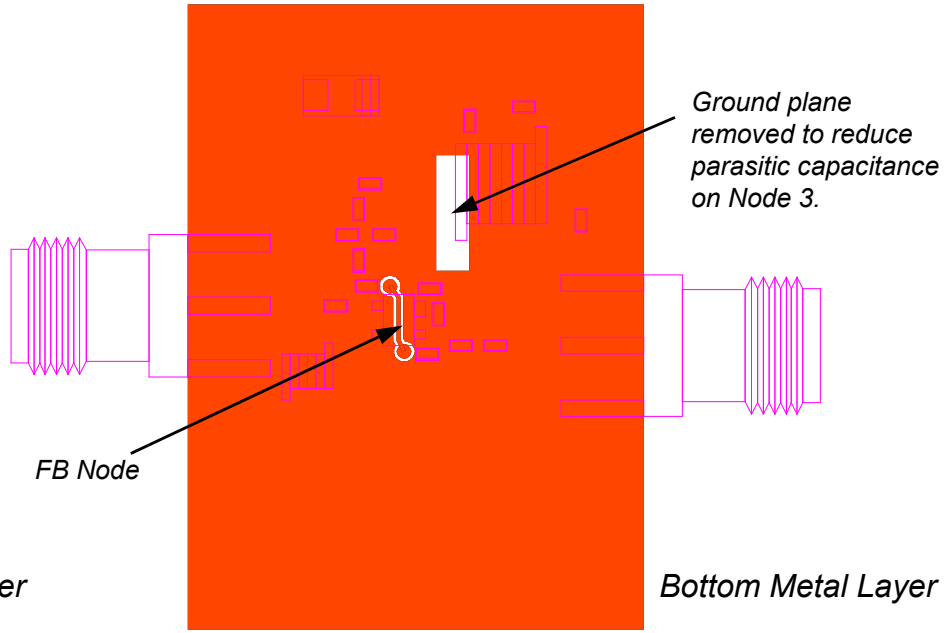
Maximum Available Gain with PCB Parasitics



- Maximum Available Gain is displayed and highlighted. The predicted maximum possible gain is around 10.8dB. This is 1.2dB below the 12dB design goal. Note that this predicted gain value is obtained with an arbitrary estimated 0.5nH of parasitic ground inductance.
- Although the gain is below the target value in these simulations, the gain without parasitic inductance is well above the target value.
- The amplifier circuit is laid out with special attention to grounding the FET source.

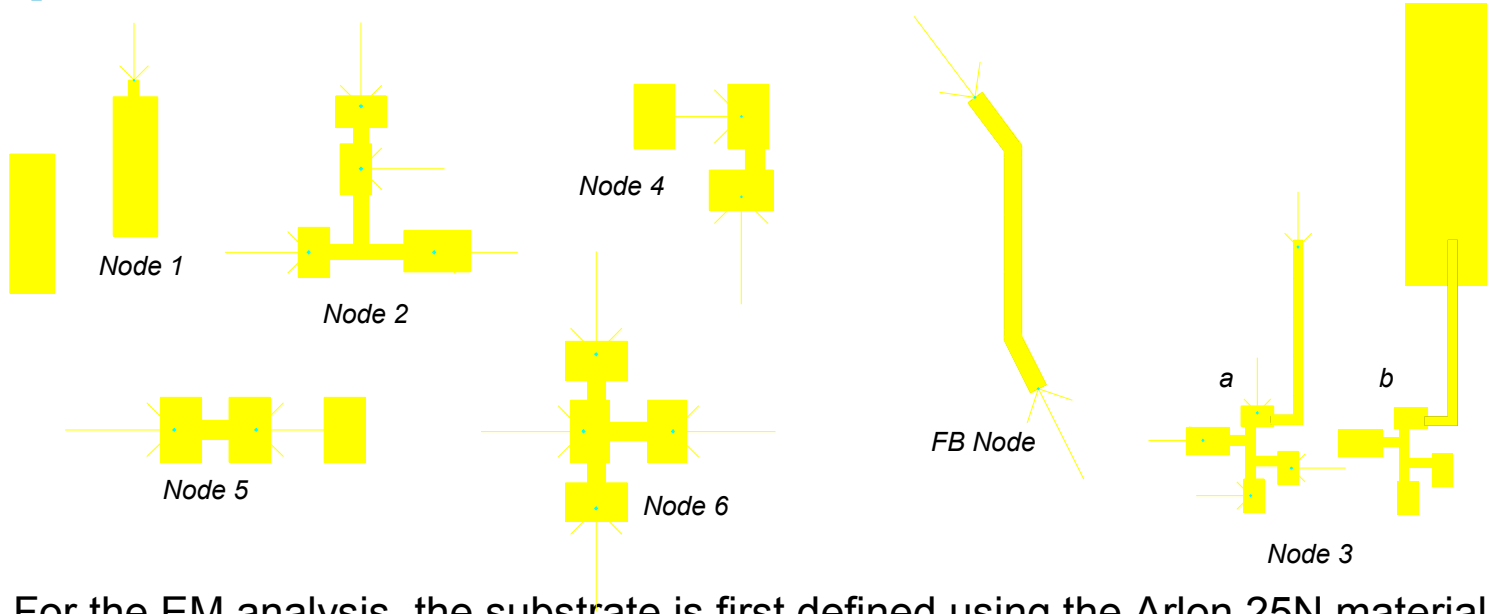
Amplifier EM/Circuit Co-Simulation & PCB Layout





- The amplifier is built on Arlon 25N, which is available in many standard laminate thicknesses. Arlon 25N has a dielectric constant of 3.38 and a loss tangent of about .0023 at 2.5GHz.
- Double-sided laminate having 1 once copper on each side, with a 30±3mil thickness is selected for the design.
- EM simulations are performed so PCB effects can be included in the circuit analysis.
- Each layout node is simulated individually and results later combined with circuit analysis to include PCB effects.

Amplifier EM/Circuit Co-Simulation & PCB Layout

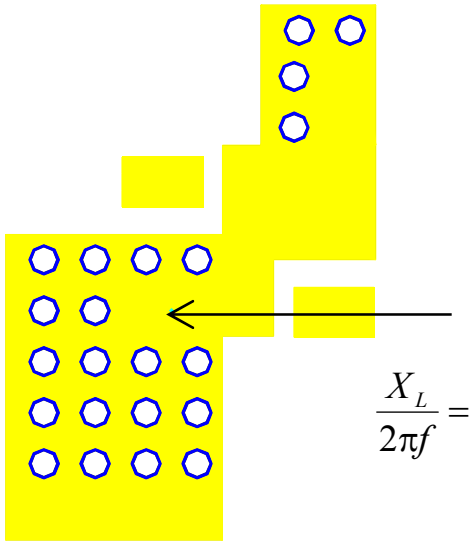


• For the EM analysis, the substrate is first defined using the Arlon 25N material properties and simulated from 10MHz to 10GHz. Once the substrate is computed, it is used for all PCB parasitic simulations.

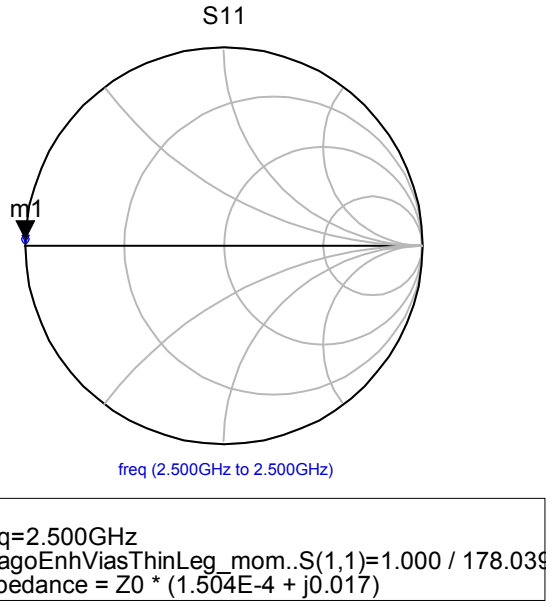
• Each RF critical layout node is simulated individually and results combined with a circuit analysis to include PCB effects. The EM/Circuit Co-Simulation feature in ADS is then employed to combine the EM results with the circuit simulation.

• The footprint pad of the 27nH choke inductor is quite large on Node 3 and adds parasitic capacitance, which in turn, lowers the inductive self-resonant frequency. Since there would be a substantial amount of parasitic capacitance on this pad, it was decided that the ground plane would be removed from beneath this pad on the bottom layer.

Amplifier EM/Circuit Co-Simulation & PCB Layout

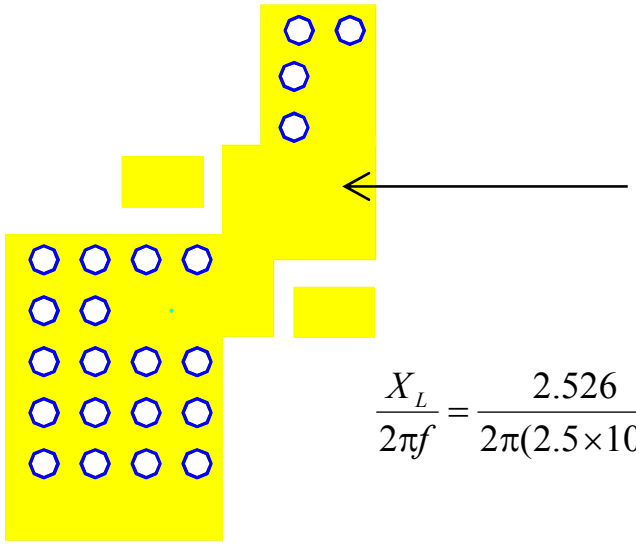


$$\frac{X_L}{2\pi f} = \frac{0.85}{2\pi(2.5\times10^9)} = 0.0541nH$$

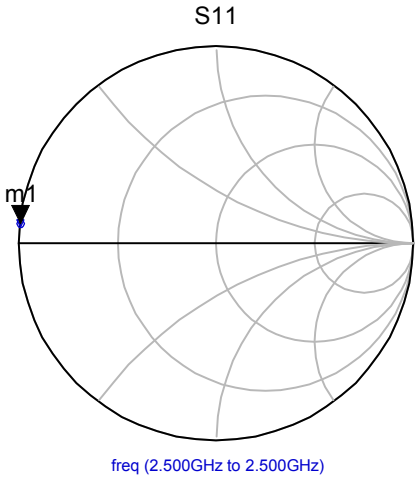


- An estimate of parasitic ground inductance on the transistor source leads is simulated.
- The transistor has two source leads that are connected internally to each other. For the parasitic ground inductance estimate, an EM simulation is performed at the connection point of each transistor source lead on the PCB.
- Since the transistor s-parameter data uses a two-port representation that has only one ground reference, the inductance value estimates for the two lead connections are combined as parallel inductances to obtain one parasitic ground inductance value.
- Inductive reactance is j(50×0.017)=j0.85, which is less than half of the parasitic inductive reactance from the first case, as shown on the Smith chart marker readout.

Amplifier EM/Circuit Co-Simulation & PCB Layout



$$\frac{X_L}{2\pi f} = \frac{2.526}{2\pi(2.5\times10^9)} = 0.1608nH$$



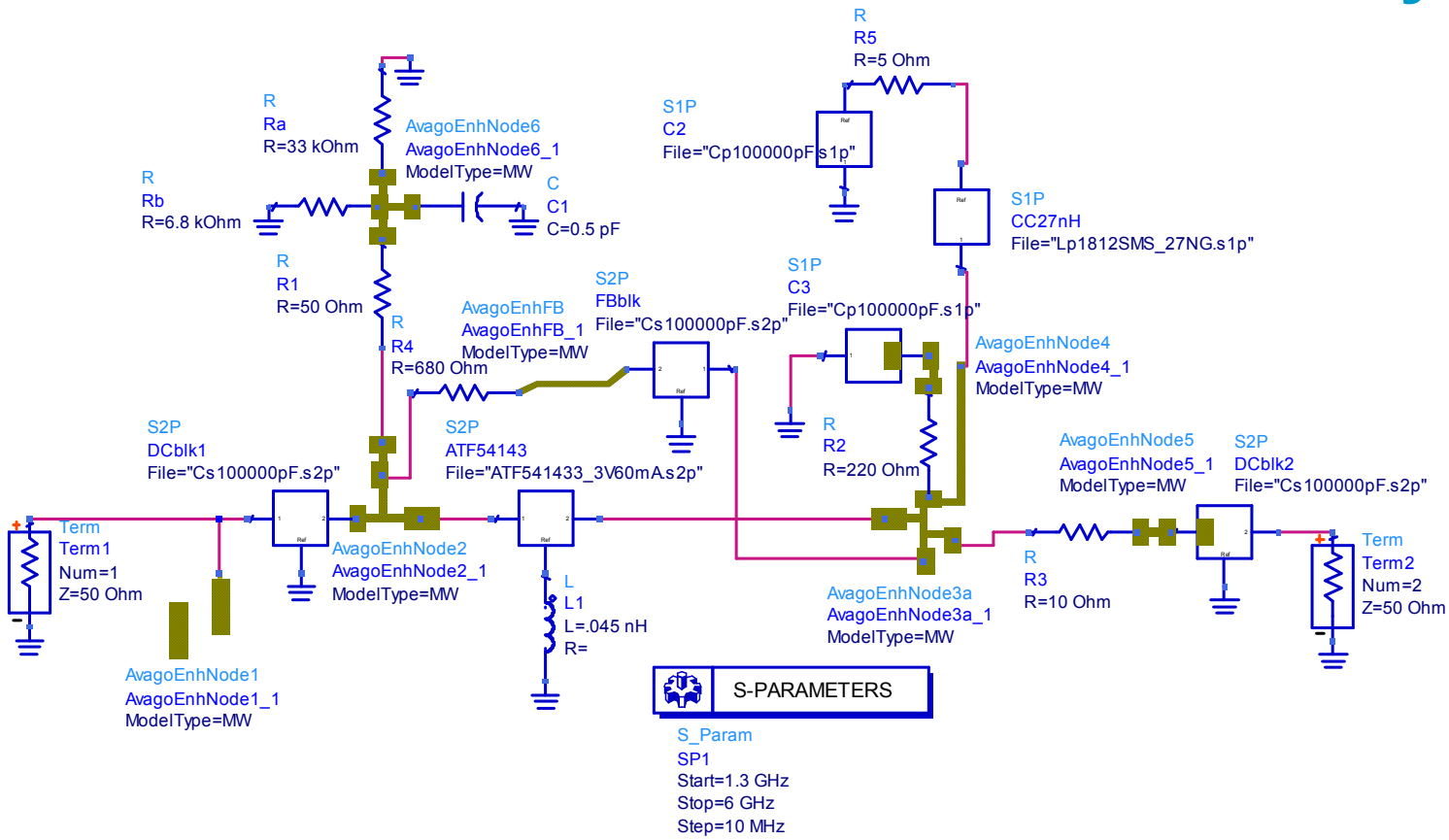
m1
freq=2.500GHz
AvagoEnhViasWideLeg_mom..S(1,1)=0.999 / 174.213
impedance = Z0 * (3.199E-4 + j0.051)

• Inductive reactance is j(50×0.0505)=j2.526 as shown on the Smith chart marker readout.

• The two calculated inductance values of 0.05447nH and 0.1608nH are now put in parallel to obtain an estimate of parasitic inductance. Note that putting the inductance values in parallel with each other is a very crude approach, but will likely give a decent ballpark estimate of parasitic ground inductance. Putting the inductances in parallel yields an estimated parasitic ground inductance of 0.045nH.

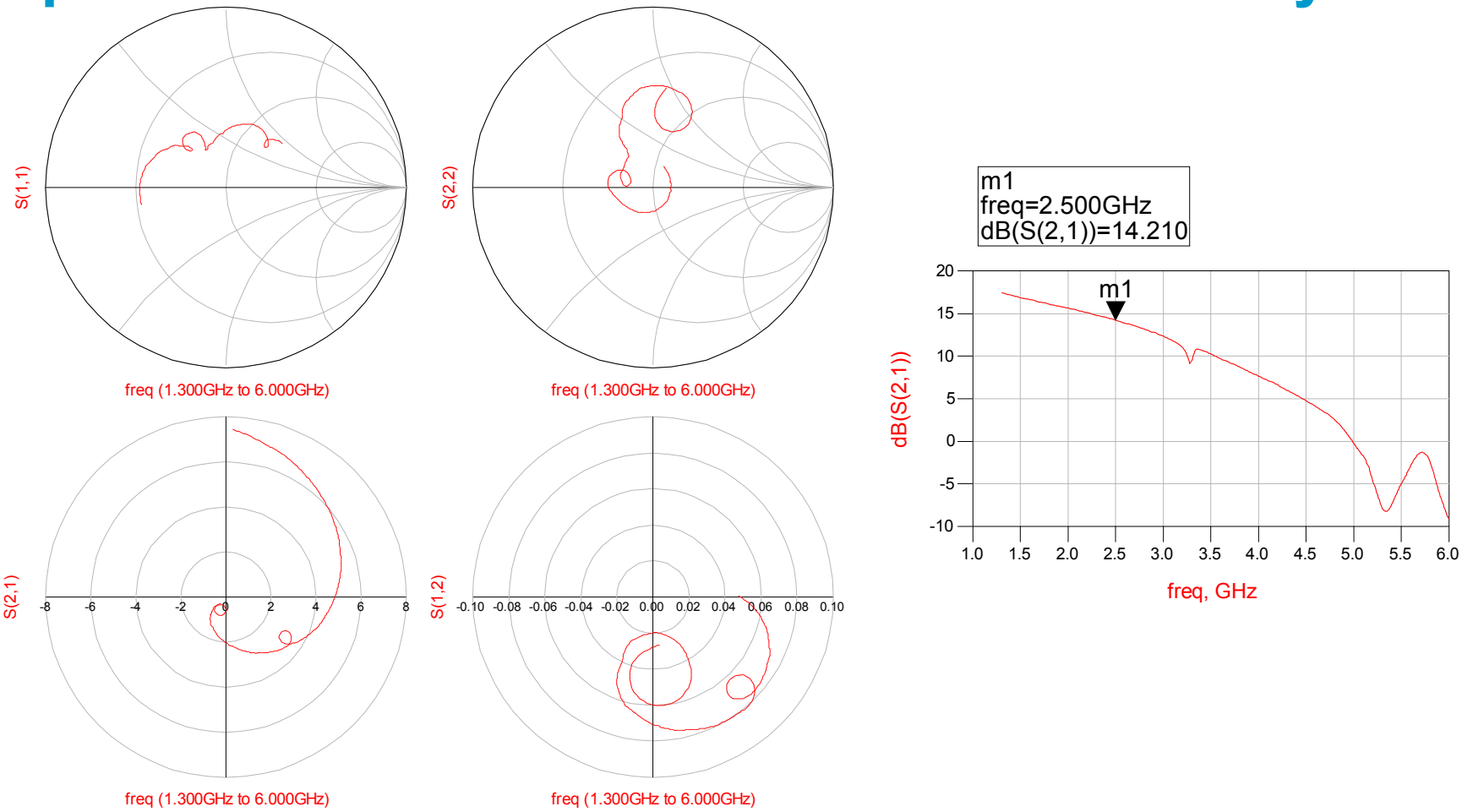
• An alternate approach to putting the inductance values in parallel would be to use the nonlinear model for the simulation since it includes both source leads.

Amplifier EM/Circuit Co-Simulation & PCB Layout



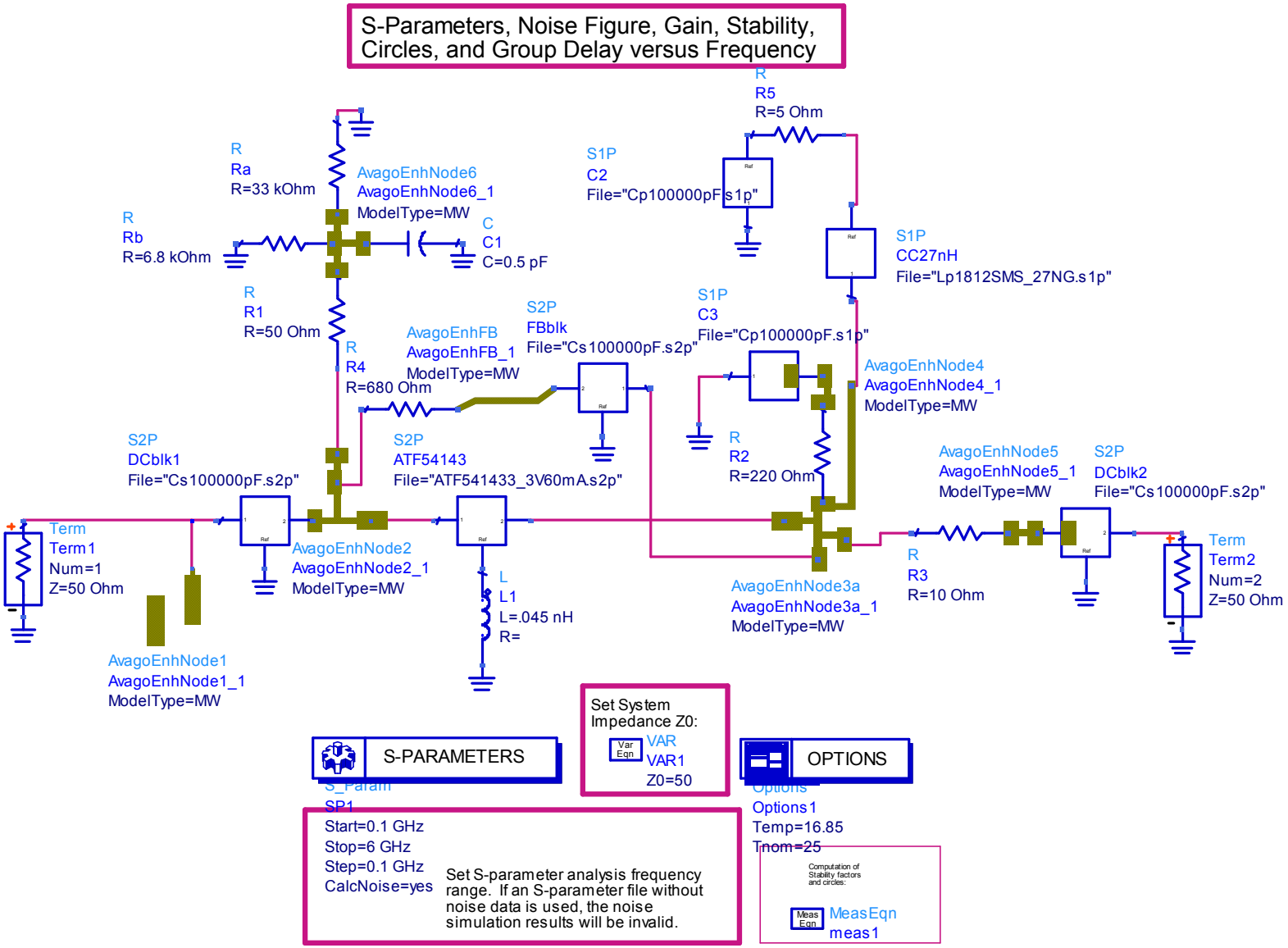
- The PCB layout node of each PCB layout trace is combined with the circuit component models and measured data to EM/Circuit Co-Simulate the entire circuit with layout parasitics.
- Measured data for the 0.1uF capacitor is included for the DC blocking capacitors and DC bypassing capacitors.

Amplifier EM/Circuit Co-Simulation & PCB Layout

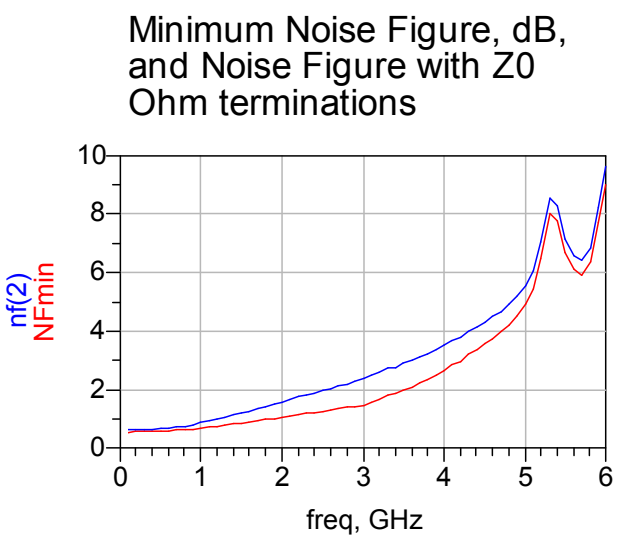


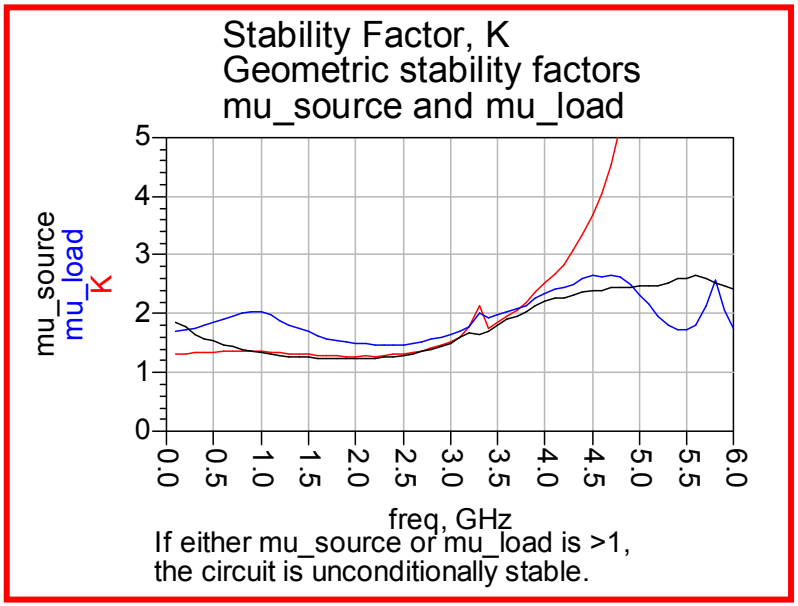
Note that the input matching network is not yet included in the schematic. It is useful to analyze amplifier stability results without matching networks since matching networks can decouple the gain block from the measurement system at some frequencies when series reactances increase toward infinity.

Stability with PCB Using EM/Circuit Co-Simulation



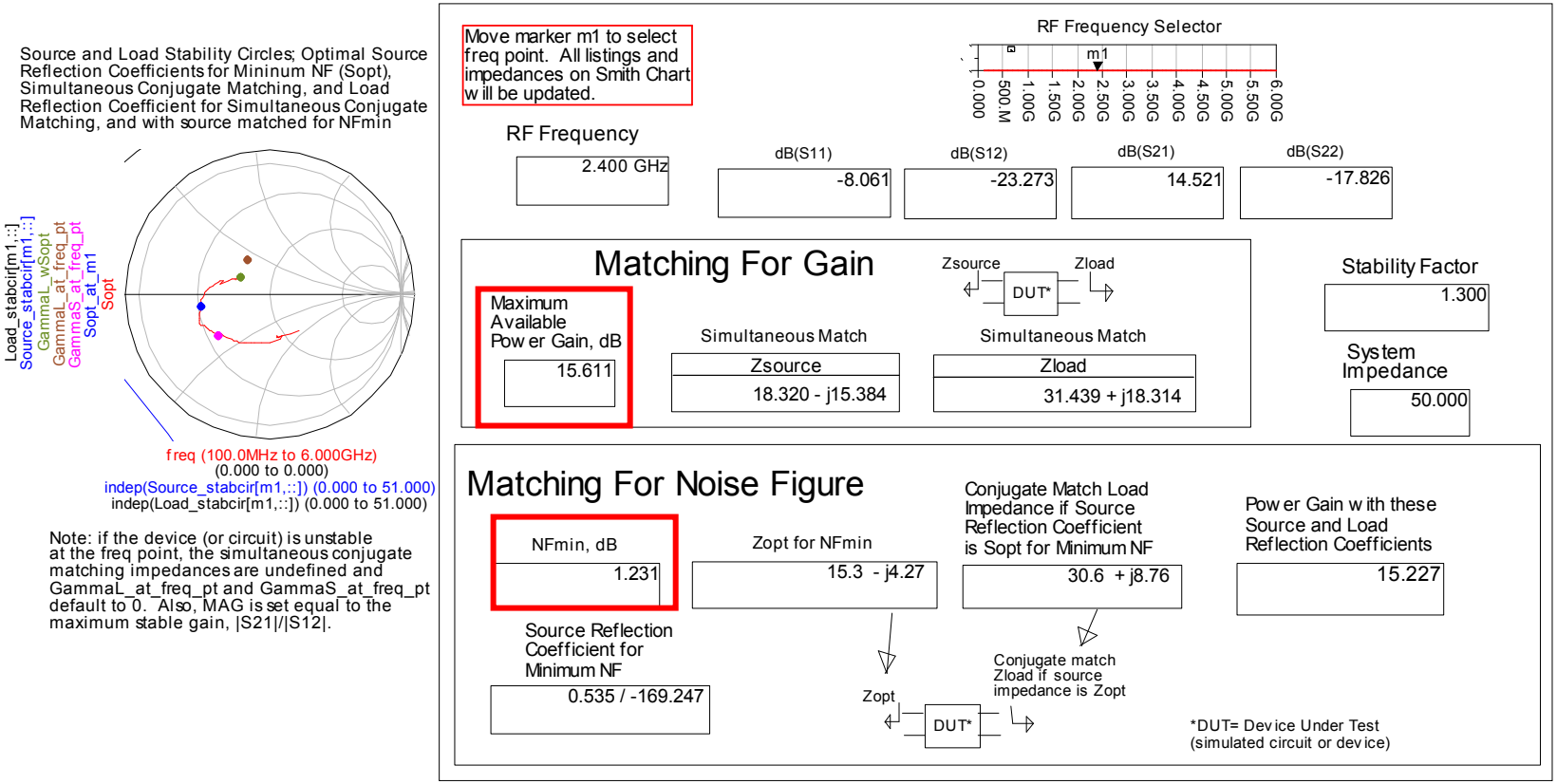
Stability with PCB Using EM/Circuit Co-Simulation





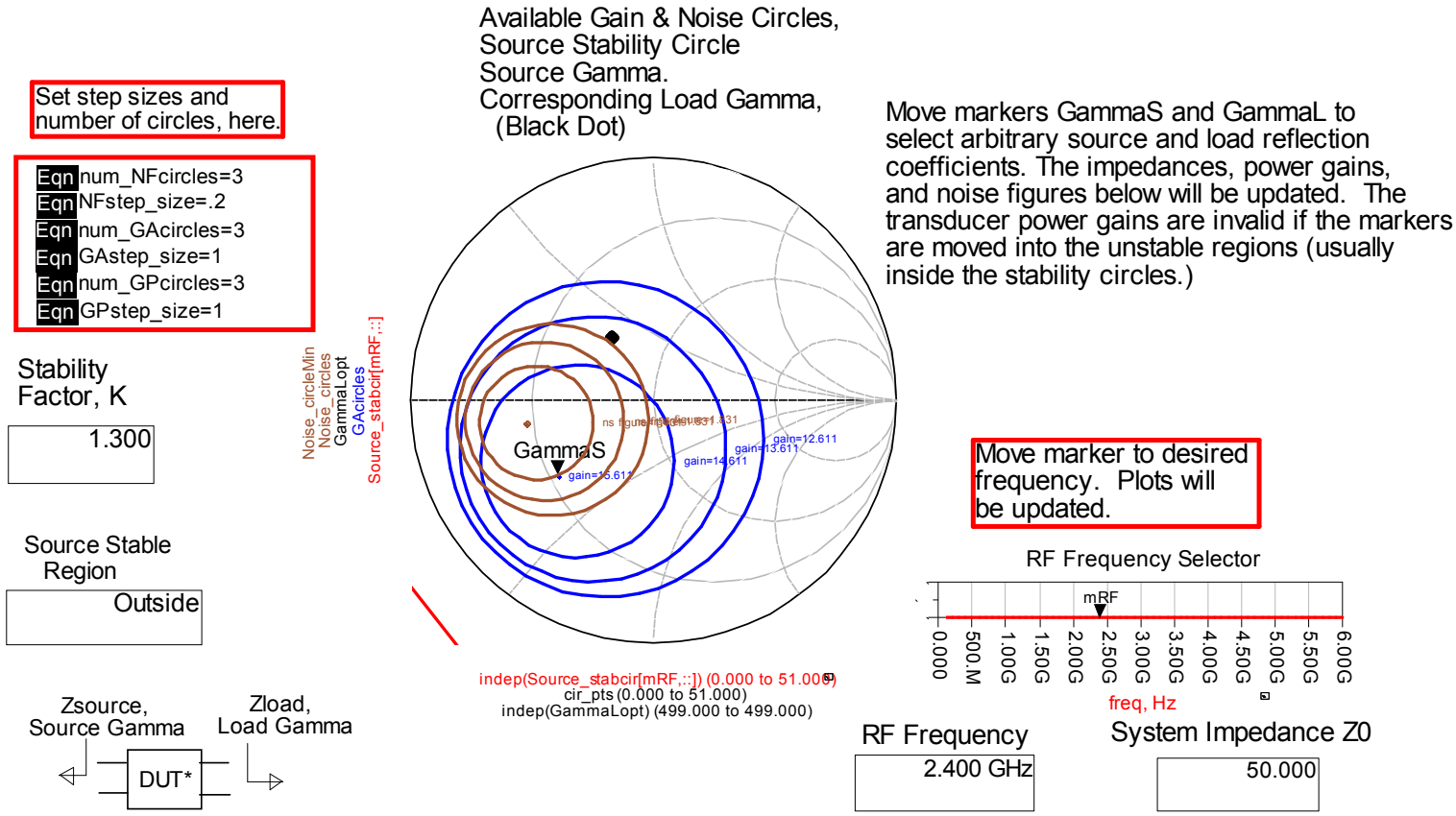
- The stability analysis is limited from 100MHz to 6GHz since the choke inductor measured data is limited to 6GHz.
- Note that $\mu_{Source} \geq 1$ and $\mu_{Load} \geq 1$ for all frequencies from 100MHz to 6GHz, either of which, guarantee unconditional stability over that frequency range.

Maximum Gain/Minimum Noise Figure



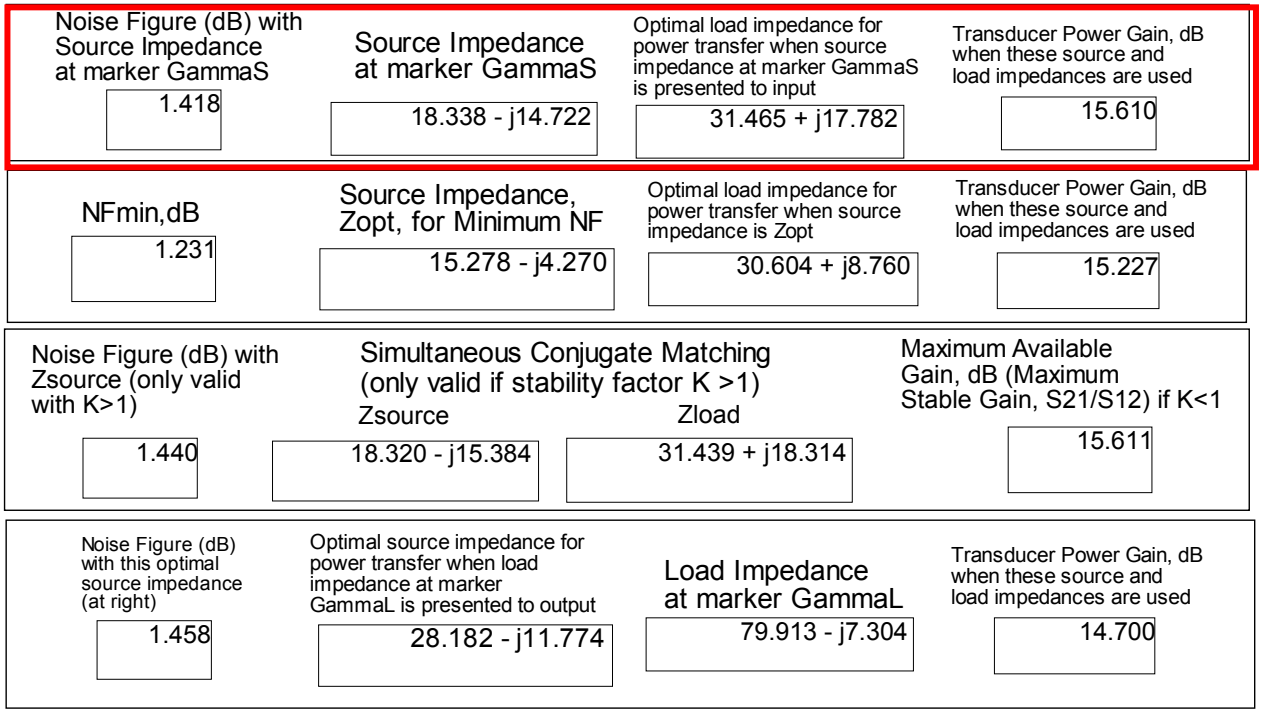
- Maximum Available Gain is 15.6dB if the input and output is presented with simultaneous conjugate match terminations.
- Minimum Noise Figure is 1.2dB if the input is presented with Γ_{opt}.

Available Gain Design Procedure



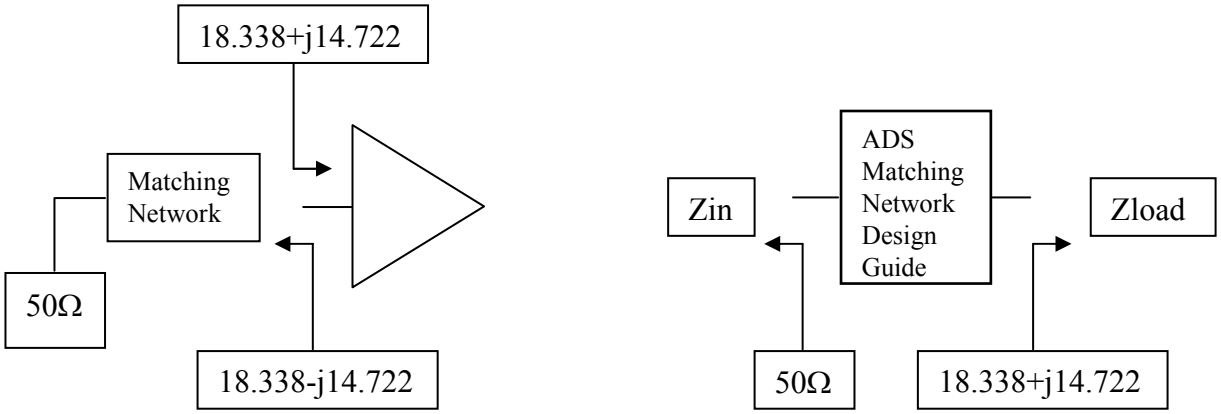
Available gain circles are plotted with noise circles. The minimum noise figure, NFmin, is 1.23dB. The first noise circle is 0.2dB higher than NFmin, or 1.4dB. The 1.4dB noise circle passes right through Γ_{MS}, the simultaneous conjugate input match. Thus, the marker is moved to the 1.4dB noise figure circle at Γ_{MS}.

Available Gain Design Procedure



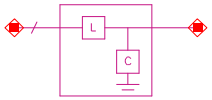
The marker readout shows the impedance that must be presented to the amplifier input to achieve 1.42dB noise figure and 15.6dB of gain. The 18.338-j14.722 impedance is what the amplifier input “wants to see” to obtain these results. It is also assumed that the output will be conjugately matched when the amplifier input is terminated with this impedance. In reality, the amplifier output doesn’t require much output matching since it’s output reflection coefficient is already pretty low. Thus, the last step of the available gain design procedure, which is to conjugately match the output for the given source termination, will not be executed. The expected gain of 15.6dB will not be reached, but will be reduced by a very small amount.

Available Gain Design Procedure (Input Match)



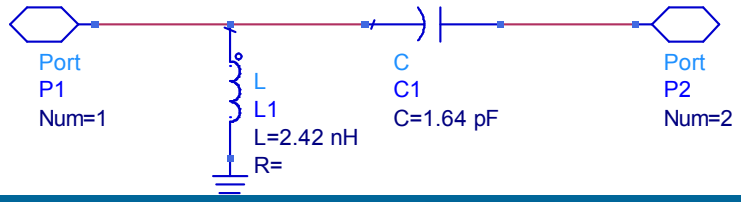
The input match must transform 50Ω to 18.338-j14.722 at 2.5GHz. An ADS Matching Design Guide is used to develop the matching network. The Design Guide assumes that one impedance is being matched to another impedance, whereas, the marker readout on the previous slide is what the amplifier input "wants to see". Notice how the reference is changed from what the amplifier "wants to see" at its input to how the ADS Matching Network Design Guide is configured.

Lumped Element Match Design Assistant
Need Help? Please see the appropriate DesignGuide User Manual

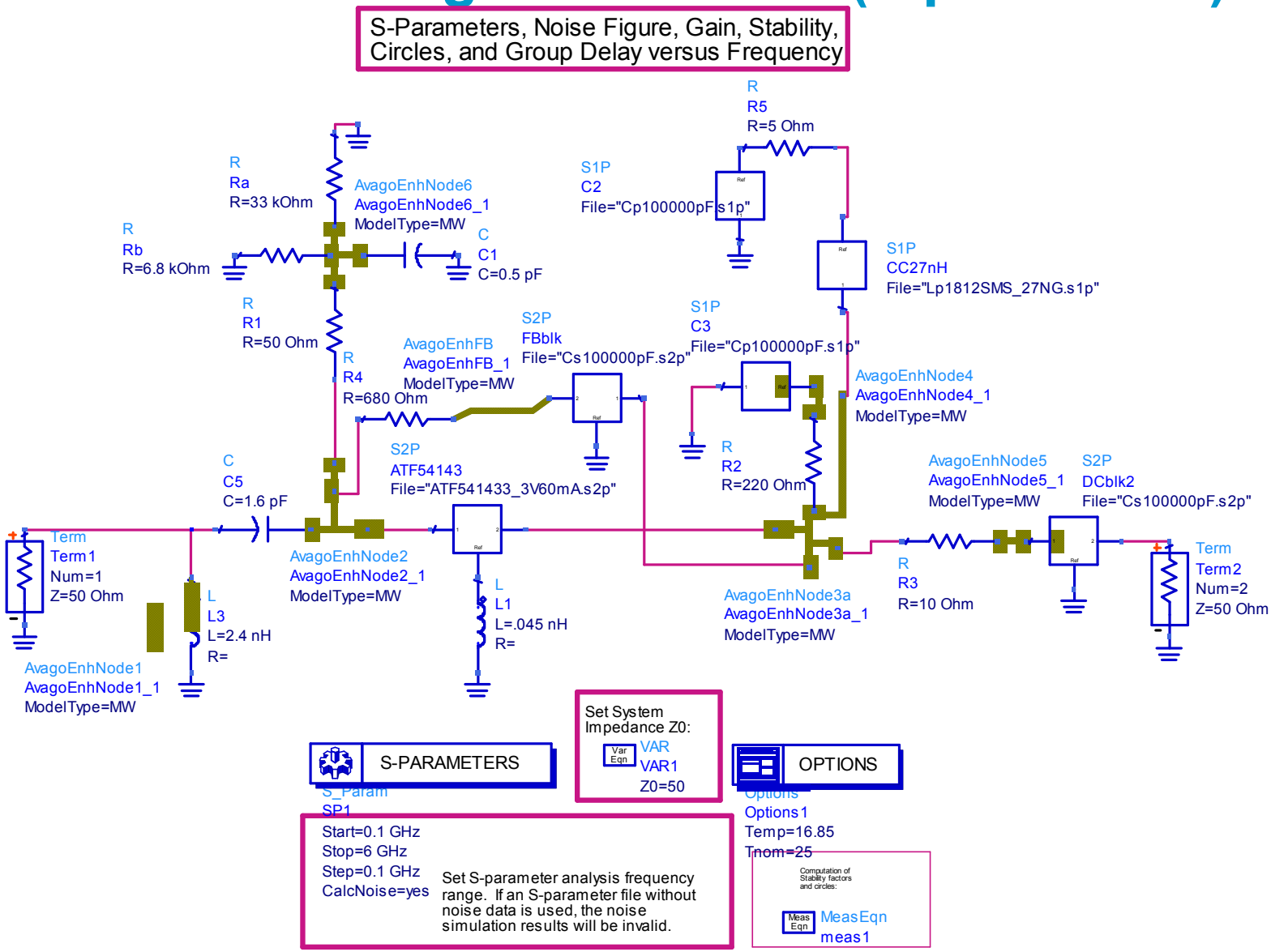


DA_LEMatch1_untitled1
DA_LEMatch1
F=2.5 GHz
Zin=50 Ohm
Zload=18.338+j*14.722 Ohm

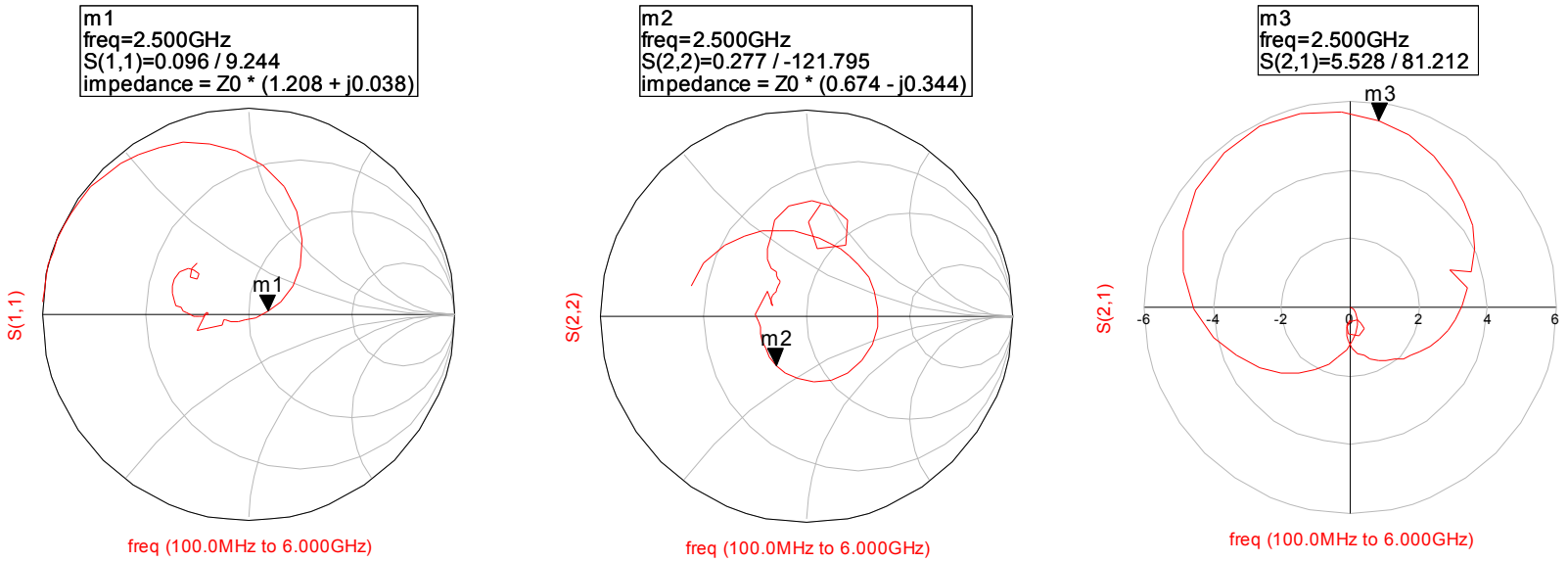
VAR
VAR1
Parameters="#2.5 GHz#50 Ohm#18.338+j*14.722 Ohm#0"



Available Gain Design Procedure (Input Match)

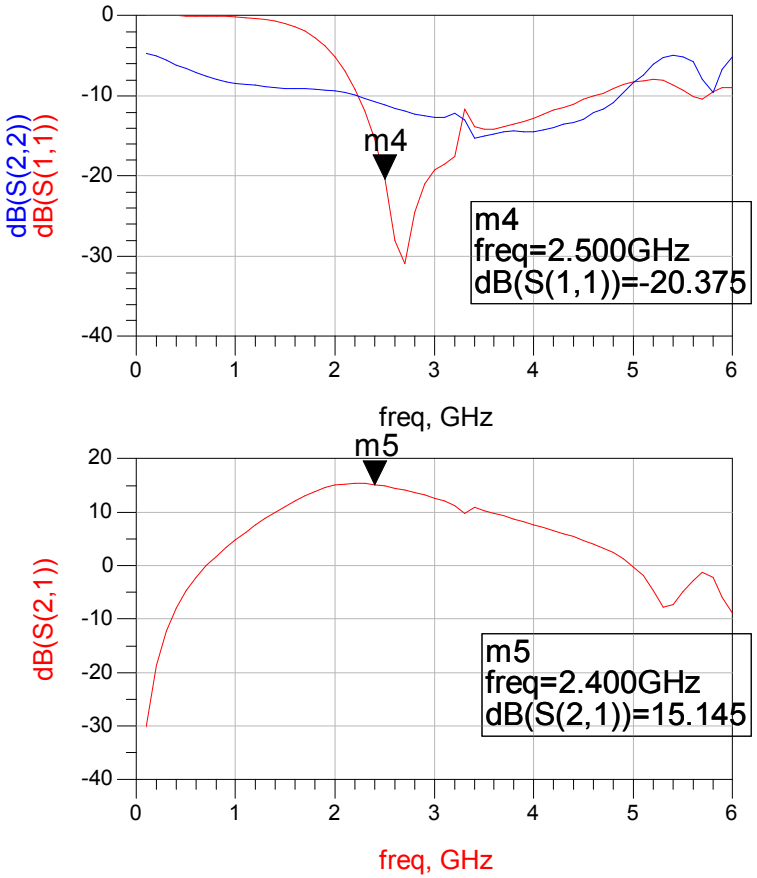


Available Gain Design Procedure (Input Match)



- The Smith charts indicate both the input and output are well matched at 2.5GHz.
- The numeric gain on the S21 polar chart at 2.5GHz is 5.53, which converts to 14.85dB.
- (The inductor is not connected to the inductor pad from the Node1 EM simulation since the first Node1 EM simulation is a one-port s-parameter dataset.)

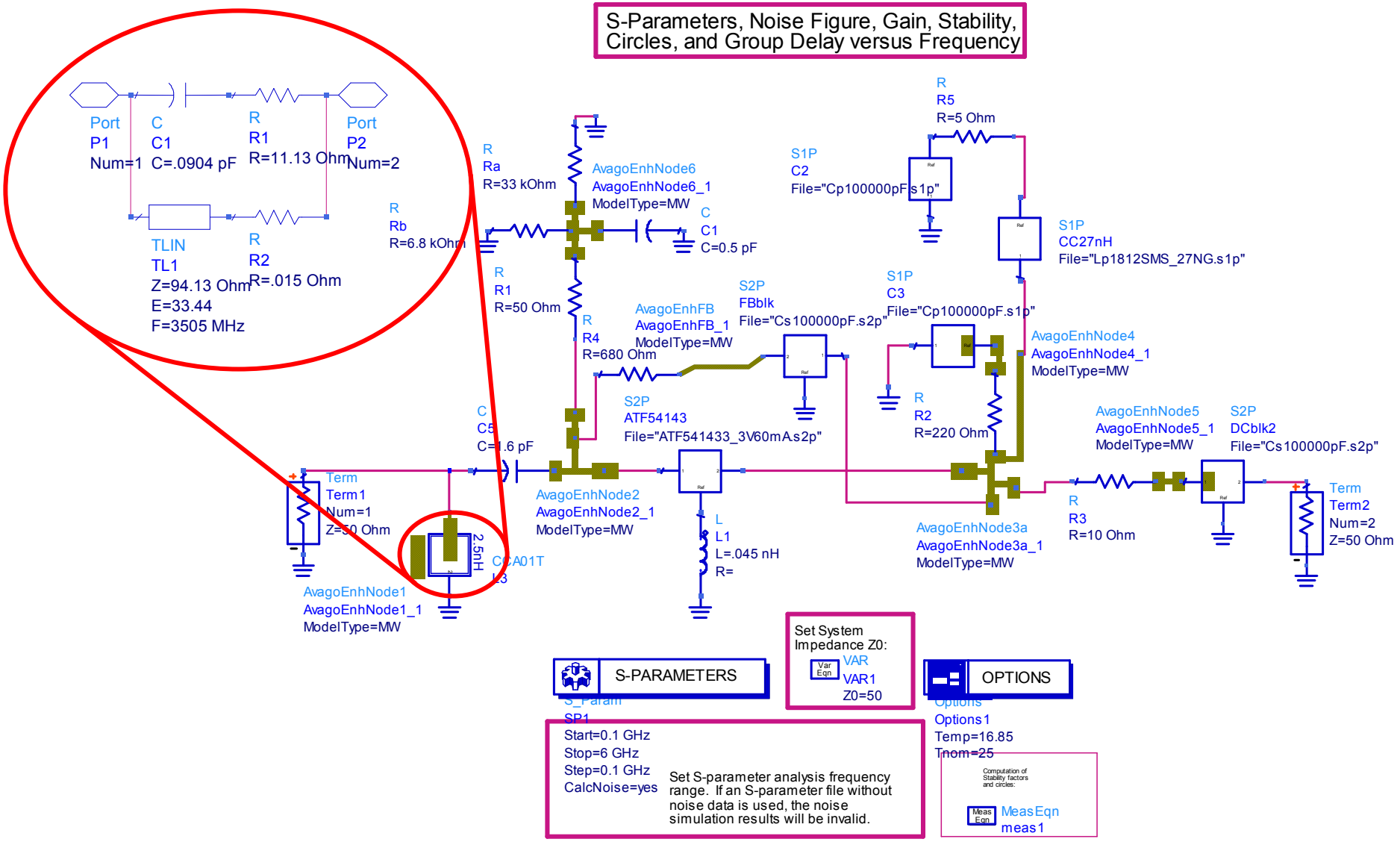
Available Gain Design Procedure (Input Match)



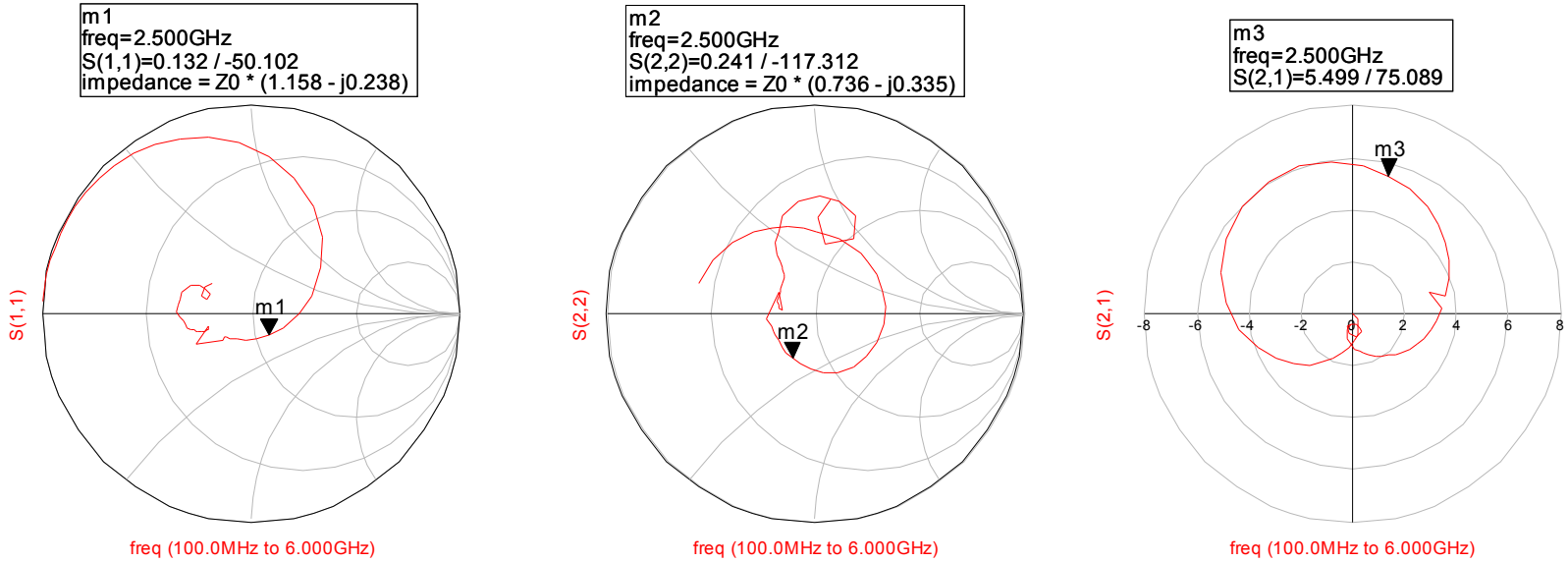
freq	nf(2)
100.0 MHz	46.633
200.0 MHz	34.725
300.0 MHz	27.837
400.0 MHz	23.017
500.0 MHz	19.338
600.0 MHz	16.396
700.0 MHz	13.968
800.0 MHz	11.931
900.0 MHz	10.002
1.000 GHz	8.925
1.100 GHz	7.709
1.200 GHz	6.655
1.300 GHz	5.739
1.400 GHz	4.944
1.500 GHz	4.257
1.600 GHz	3.669
1.700 GHz	3.169
1.800 GHz	2.752
1.900 GHz	2.410
2.000 GHz	2.151
2.100 GHz	1.937
2.200 GHz	1.776
2.300 GHz	1.666
2.400 GHz	1.599
2.500 GHz	1.562
2.600 GHz	1.562
2.700 GHz	1.593
2.800 GHz	1.650
2.900 GHz	1.730
3.000 GHz	1.829

- A gain of 15.15dB at 2.4GHz is plotted on the rectangular plot. A 20dB input return loss and 10dB output return loss are also plotted.
- The predicted noise figure with the input match is 1.6dB at 2.4GHz and 1.56dB at 2.5GHz.

Available Gain Design Procedure (Input Match)

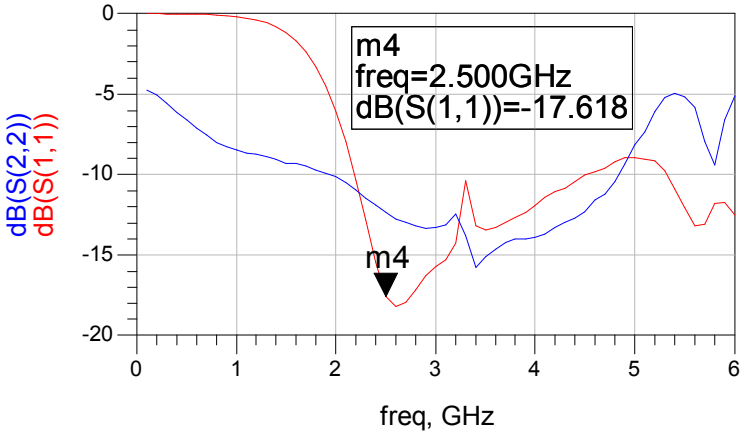


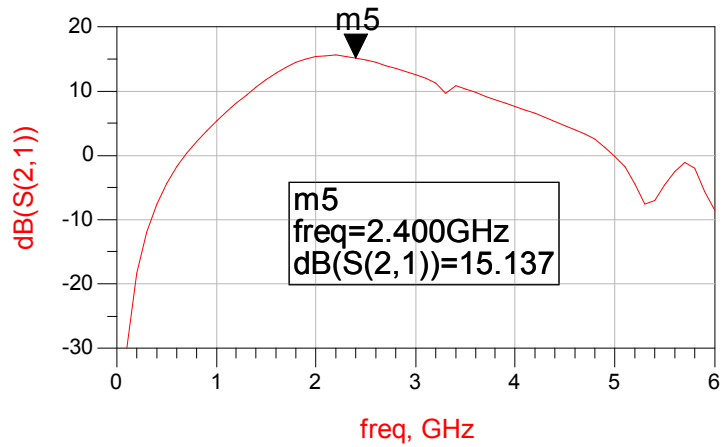
Available Gain Design Procedure (Input Match)



- A 2.4nH Coilcraft airwound inductor is available for the input matching network.
- The lumped equivalent 2.4nH Coilcraft inductor replaces the L3 ideal inductor.
- S11 and S22 Smith chart plots indicate that both input and output are very well matched.

Available Gain Design Procedure (Input Match)

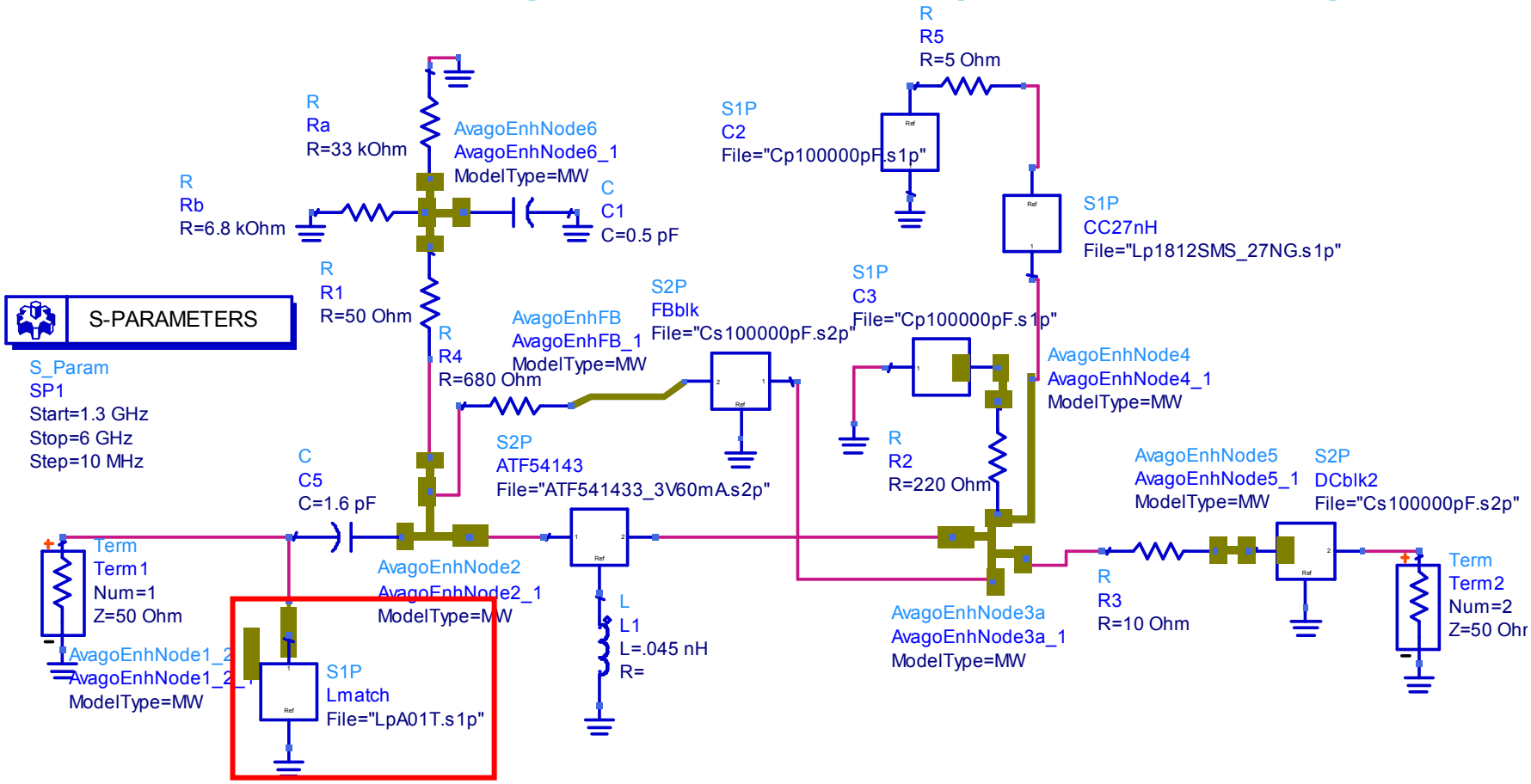




freq	nf(2)
100.0 MHz	46.297
200.0 MHz	34.385
300.0 MHz	27.488
400.0 MHz	22.656
500.0 MHz	18.964
600.0 MHz	16.007
700.0 MHz	13.565
800.0 MHz	11.513
900.0 MHz	9.574
1.000 GHz	8.483
1.100 GHz	7.261
1.200 GHz	6.206
1.300 GHz	5.296
1.400 GHz	4.514
1.500 GHz	3.848
1.600 GHz	3.288
1.700 GHz	2.825
1.800 GHz	2.451
1.900 GHz	2.157
2.000 GHz	1.950
2.100 GHz	1.788
2.200 GHz	1.681
2.300 GHz	1.622
2.400 GHz	1.605
2.500 GHz	1.616
2.600 GHz	1.658
2.700 GHz	1.726
2.800 GHz	1.816
2.900 GHz	1.924
3.000 GHz	2.046

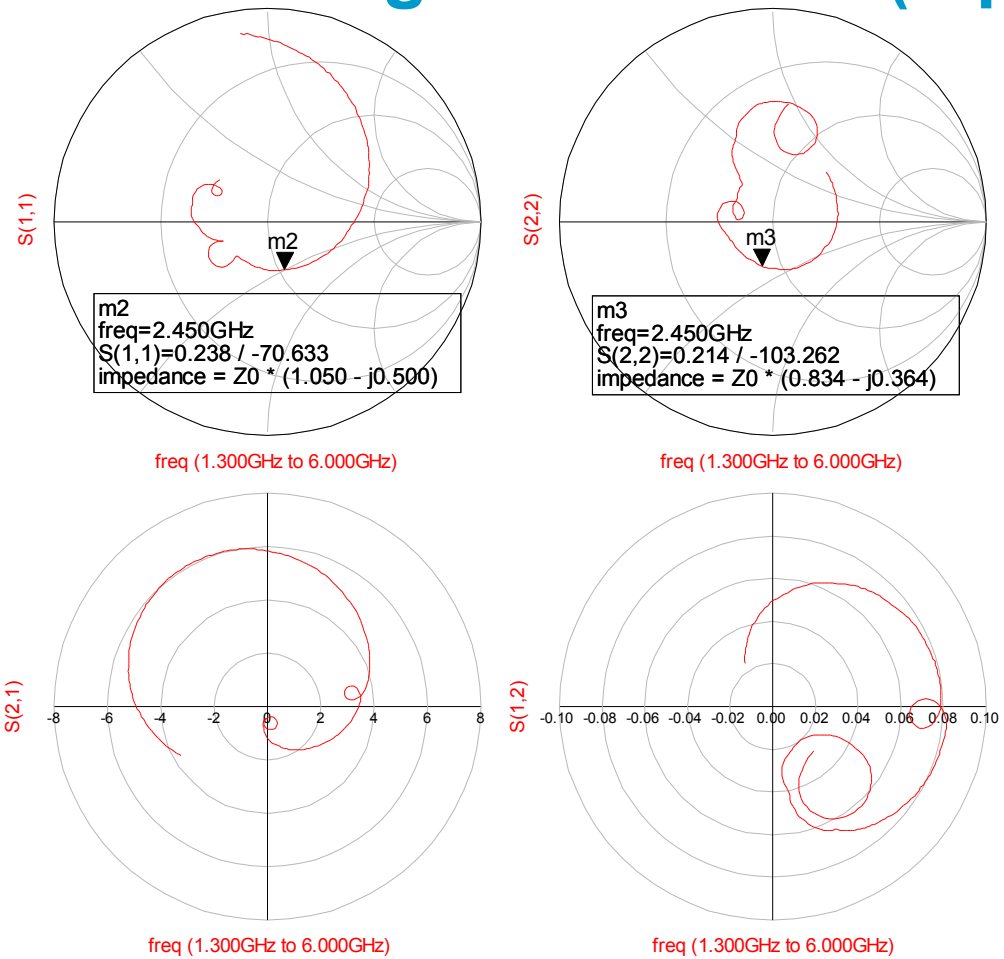
- The input return loss with the inductor model plotted in Figure 59 shows a slight degradation from 20dB to 17.6dB.
- The 15.14dB gain is unaffected by the slight input return loss degradation.
- The 2.4nH coil loss slightly degrades noise figure to 1.62dB.

Available Gain Design Procedure (Input Match)



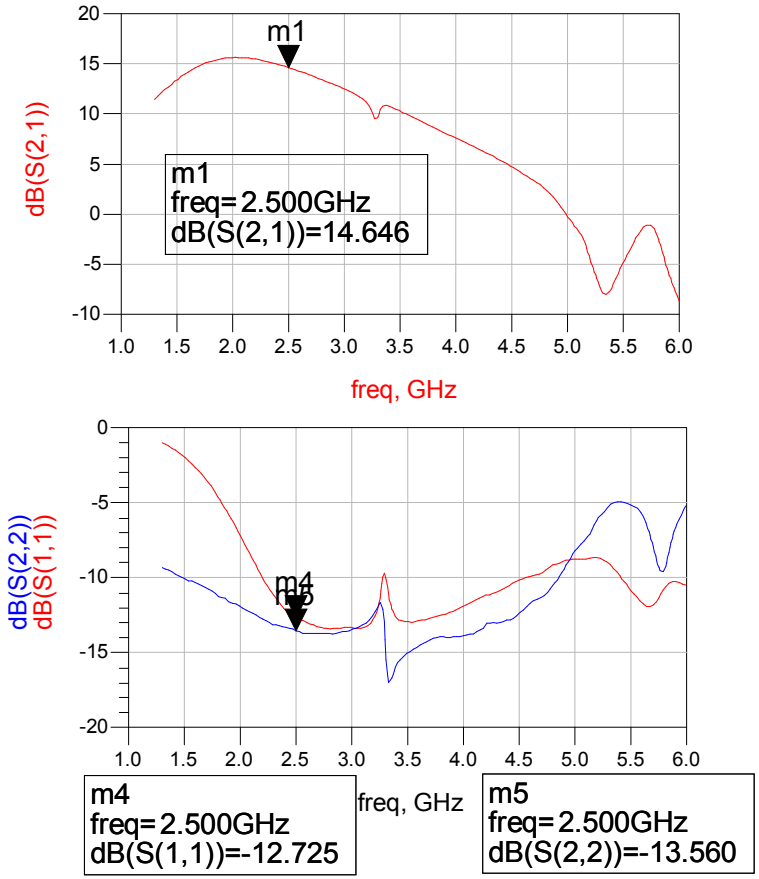
- The Node1 one-port s-parameter EM simulated dataset is replaced by the two-port s-parameter data so that the lumped equivalent circuit model is connected correctly to the PCB trace pad.
- The 2.4nH Coil Craft equivalent circuit model is replaced by one-port measured data.

Available Gain Design Procedure (Input Match)



The measured data for the 2.4nH input matching inductor indicates that the lumped equivalent model under-estimates loss of the actual inductor since gain degrades from 15.137dB to 14.65dB and noise figure degrades from 1.6dB to 1.78dB at 2.5GHz.

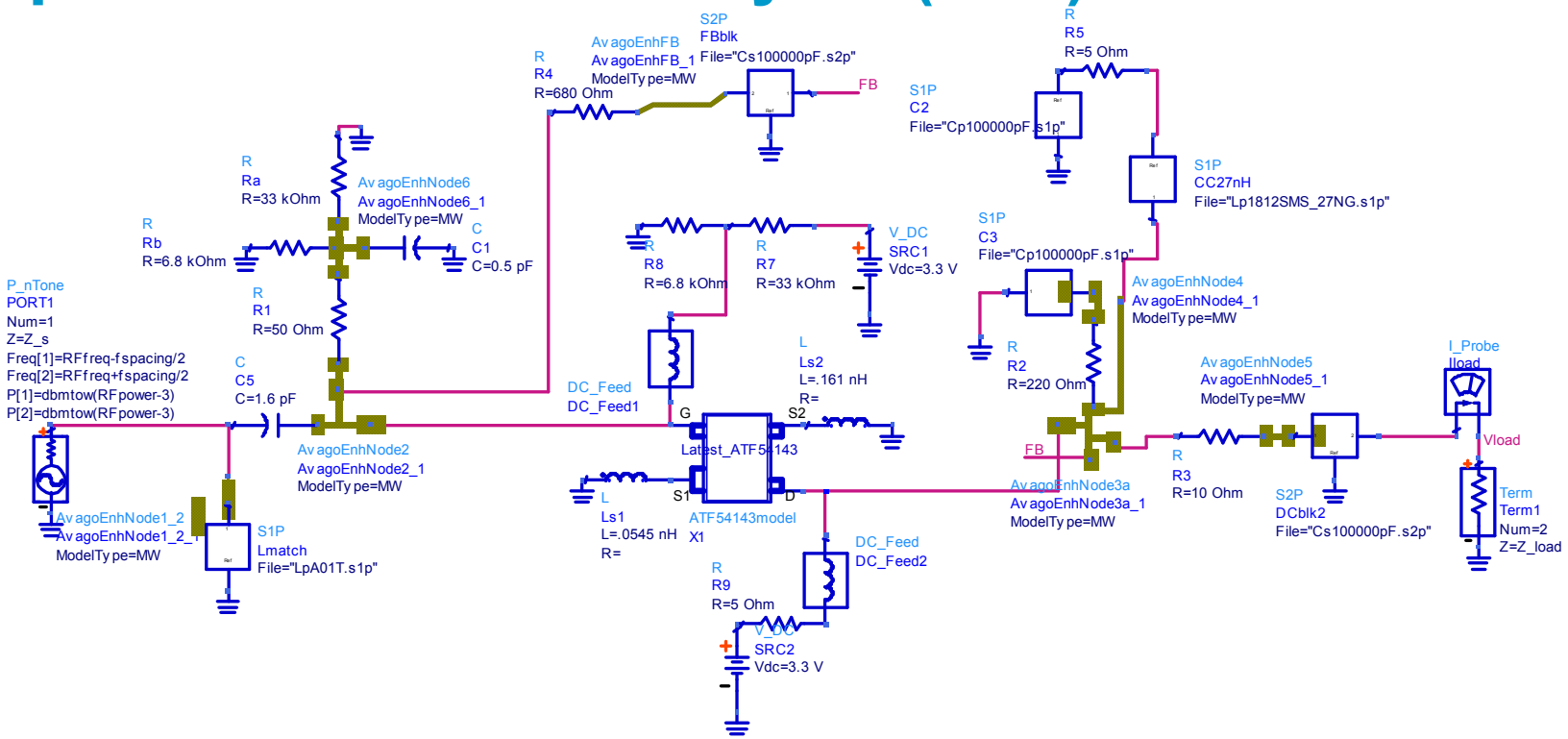
Available Gain Design Procedure (Input Match)



freq	nf(2)
2.370 GHz	1.725
2.380 GHz	1.729
2.390 GHz	1.730
2.400 GHz	1.731
2.410 GHz	1.736
2.420 GHz	1.738
2.430 GHz	1.743
2.440 GHz	1.748
2.450 GHz	1.753
2.460 GHz	1.758
2.470 GHz	1.763
2.480 GHz	1.768
2.490 GHz	1.774
2.500 GHz	1.779
2.510 GHz	1.785
2.520 GHz	1.792
2.530 GHz	1.799
2.540 GHz	1.806
2.550 GHz	1.815
2.560 GHz	1.821
2.570 GHz	1.831
2.580 GHz	1.840
2.590 GHz	1.846
2.600 GHz	1.853
2.610 GHz	1.864
2.620 GHz	1.867
2.630 GHz	1.875

Input return loss degrades from 17.6dB to 12.7dB using the inductor measured data versus the equivalent circuit model.

Amplifier Nonlinear Analysis (IMD)



HARMONIC BALANCE

```
HarmonicBalance
HB1
MaxOrder=Max_IMD_order
Freq[1]=RFfreq-fspacing/2
Freq[2]=RFfreq+fspacing/2
Order[1]=7
Order[2]=7
UseKrylov=yes
```

Set these values:

```
VAR
VAR1
RFfreq=2450 MHz
fspacing=5MHz
RFpower=-10 _dBm
Max_IMD_order=7
```

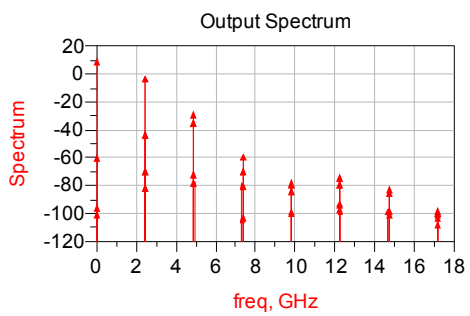
Set Load and Source impedances at baseband, fundamental and harmonic frequencies

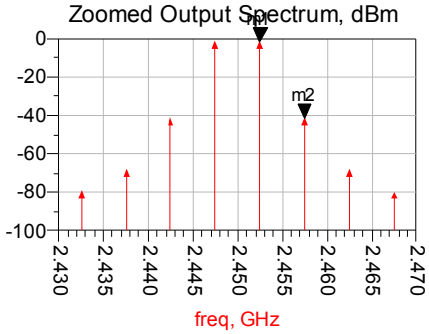
```
VAR
VAR2
Z0=50
;Load Impedaneces=
Z_l_bb=Z0+j*0
Z_l_fund = Z0 + j*0
Z_l_2 = Z0 + j*0
Z_l_3 = Z0 + j*0
Z_l_4 = Z0 + j*0
Z_l_5 = Z0 + j*0
;Source Impedances=
Z_s_bb=Z0+j*0
Z_s_fund = Z0 + j*0
Z_s_2 = Z0 + j*0
Z_s_3 = Z0 + j*0
Z_s_4 = Z0 + j*0
Z_s_5 = Z0 + j*0
```

```
VAR
global VAR6
f_bb=0.5*RFfreq
f_1 = 1.5*RFfreq
f_2 = 2.5*RFfreq
f_3 = 3.5*RFfreq
f_4 = 4.5*RFfreq
```

Two-Tone Harmonic Balance Simulation at one set of input frequencies and powers.

Amplifier Nonlinear Analysis (IMD)





Equations are on the "Equations" page.

Fundamental Frequencies	Available Source Power Both Tones, dBm	Fundamental Output Power, Both Tones, dBm	Transducer Power Gain
2.447500 G 2.452500 G	-10.00	1.289	11.289

Low and High Side Output TOI Points, dBm		Low and High Side Input TOI Points, dBm	
18.303	18.264	7.014	6.975

Low and High Side Output 5thOI Points, dBm		Low and High Side Input 5thOI Points, dBm	
14.963	14.923	3.674	3.634

These become invalid as the amplifier is driven into compression. If the low and high side TOI points do not agree, try increasing the order of each tone and/or the Max_IMD_order.

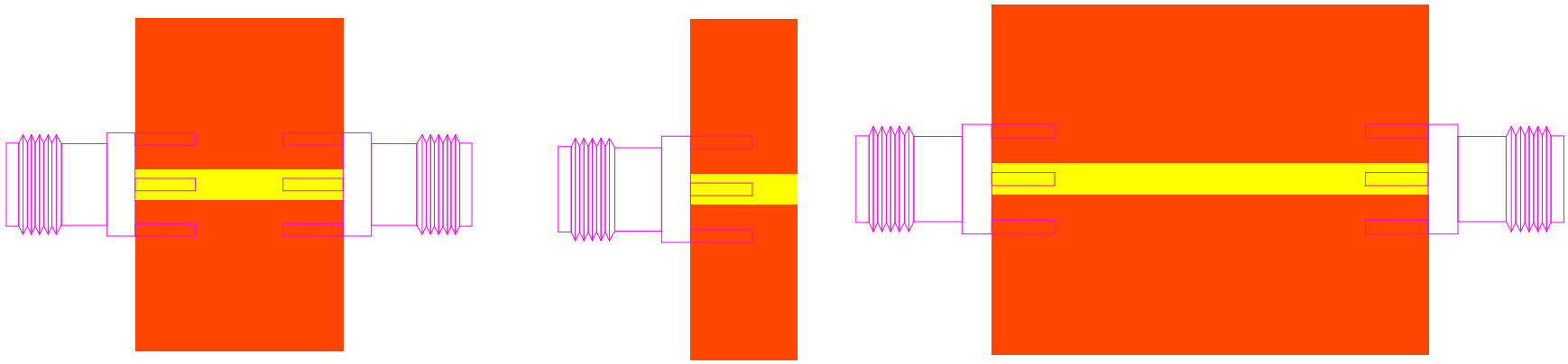
- A third order intermodulation distortion simulation is configured using the ADS Amplifier Design Guide.
- The 60 ATF54143 two-port s-parameter data is replaced in the parasitic model by the biased non-linear model.
- The red box displays a simulated third order input intercept point of 7dBm.

Simulation Results Vs. Specification Requirements

	Specification Requirement	Simulated Value
Frequency Range	2.4GHz to 2.48GHz	2.4GHz to 2.48GHz
Gain	>12dB	14.65dB
Noise Figure	<2.5dB	1.78dB
IP3i	>0dBm	7dBm
Input Return Loss	>10dB	12.7dB
Output Return Loss	>10dB	13.6dB
Current Drain	<100mA	61.38mA
Supply Voltage	3.3V	3.3V
Stability	Unconditional	Unconditional

- The simulated amplifier that includes PCB layout and component parasitics meets all amplifier design requirements.
- Since the simulated amplifier with all PCB layout and component parasitics meets or exceeds the specification requirements, the amplifier PCB is fabricated.

Arlon 25N Microstrip TRL Calibration Kit



Thru *Open (Reflect)* *Line*

$$\tau = \frac{l\sqrt{\varepsilon_r}}{c} = \frac{.0127m\sqrt{2.66}}{2.997925E8\,{}^{m}/_{\text{sec}}} = 69.1pSec$$

- Linecalc is used to design the TRL calibration standards.
- The amplifier input and output 50Ω transmission lines are 250mils long, thus, the Open standard is also 250mils long. The zero length Thru is 500mils long.
- The TRL calibration Line 1 standard is designed to cover up to 6GHz. The electrical length of the line standard is valid from 30° to 150°. Thus, the Line 1 standard should be no longer electrically than 150° at 6GHz. the Line 1 standard is the 500mil electrical length of the zero length Thru standard plus the additional Line 1 length of 500mils, yielding a total Line 1 length of 1000mils.

Arlon 25N Microstrip TRL Calibration Kit

Standard Class Assignments **Calibration Kit _____ Arlon25N**

CLASS	A	B	C	D	E	F	G	Standard Class Label
$S_{11}A$	1							Open
$S_{11}B$								
$S_{11}C$	3							Load
$S_{22}A$	1							Open
$S_{22}B$								
$S_{22}C$	3							Load
Forward Transmission	2							Thru
Reverse Transmission	2							Thru
Forward Match	2							Thru
Reverse Match	2							Thru
Response								
Response & Isolation	3							Isoln Std
TRL Thru	2							Thru
TRL Reflect	1							Open
TRL Line	4	5	6	7	8	9		Lines
Adapter								
TRL Option								
Cal Z_0: _____ System Z_0 __X___ Line Z_0								
Set Ref: ___X__ Thru _____ Reflect								

Arlon 25N Microstrip TRL Calibration Kit

Calibration Kit __ Arlon25N

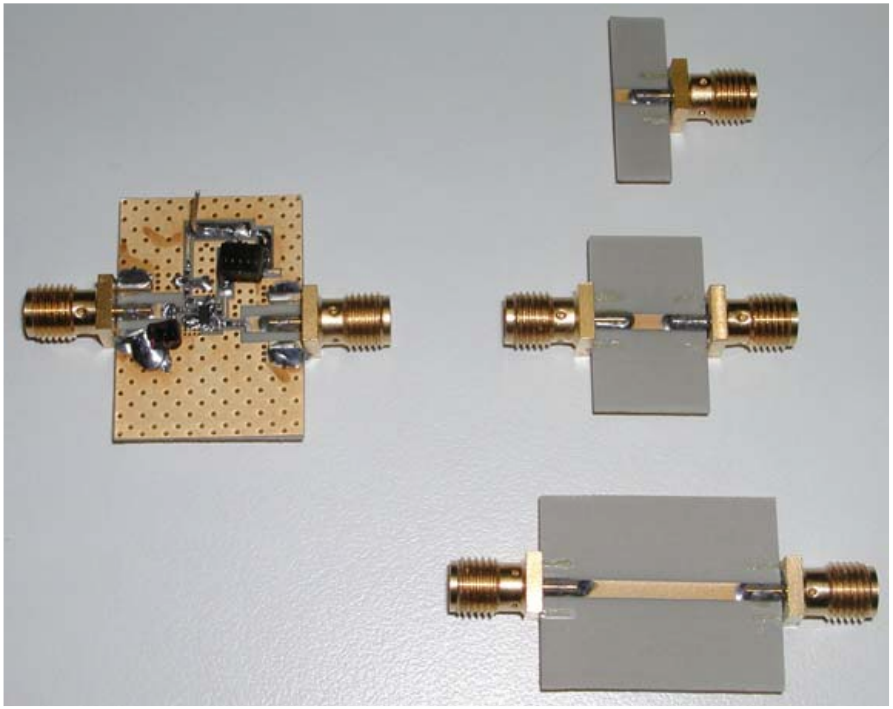
STANDARD		C0 10^{-15}F	C1 10^{-27}F/Hz	C2 10^{-36}F/Hz^2	C3 10^{-45}F/Hz^3	Fixed or Sliding	Terminal Impedance Ω	Offset			Frequency (GHz)		Coax or Waveguide	Standard Label
#	TYPE	L0 10^{-12}H	L1 10^{-24}H/Hz	L2 10^{-33}H/Hz^2	L3 10^{-42}H/Hz^3			Delay pSec	Z_0 Ω	Loss GΩ/s	MIN	MAX		
1	Open	0	0	0	0		50	0	50		0.2	20		Open
2	Thru						50	0	50		0.2	20		Thru
3	Load					Fixed	50	0	50		0.2	20		Load
4	Line 1						50	69.1	50		1.3	6		1.3-6 Line
5	Line 2						50	207.31	50		0.4	2		0.4-2 Line
6	Line 3						50	19.348	50		4.5	20		4.5-20 Line
7	Line 4						50	20.177	50		4.2	20		4.2-20 Line
8	Line 5						50	96.74	50		0.87	4.3		0.87-4.3 Line
9	Line 6						50	428.42	50		0.2	0.97		0.2-0.97 Line
10														

- The lowest frequency for the Line 1 standard that yields an electrical length of 30° is just above 1.2GHz, therefore 1.3GHz is used as the Line 1 standard lower frequency limit. Therefore, the Line 1 standard, which is physically 500mils long, covers a frequency range of 1.3GHz to 6GHz.

- The electrical delay of the Line 1 standard is 69.1pSec.

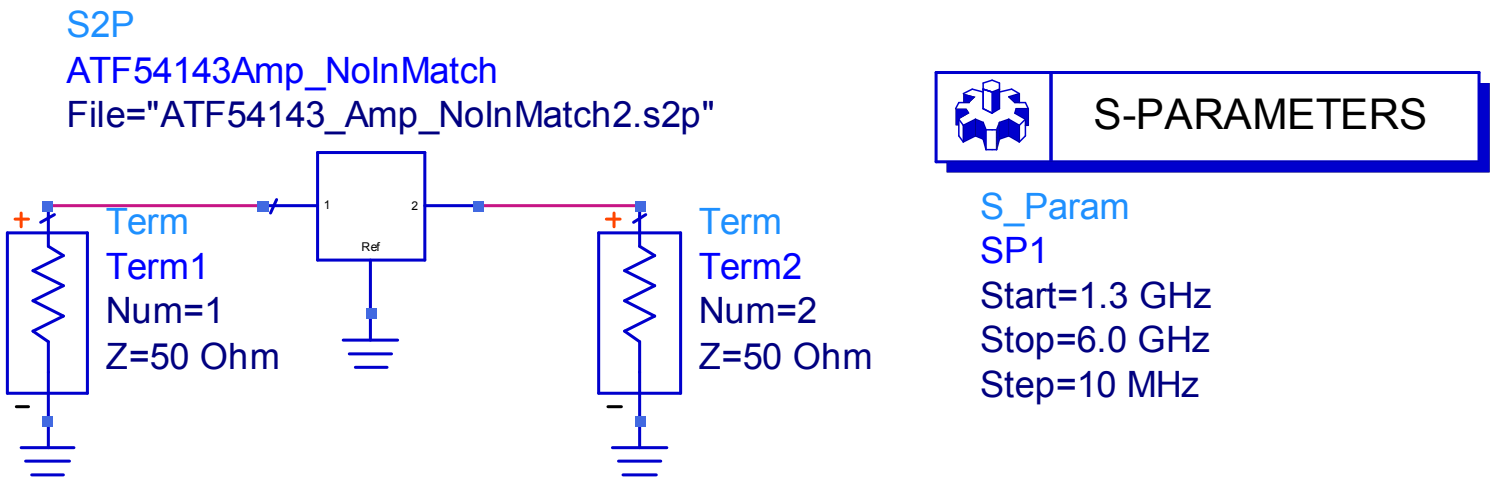
- Calibration coefficients from the table are entered into the network analyzer. The amplifier and TRL calibration standards are fabricated. The network analyzer is now calibrated using the Arlon 25N TRL calibration kit using the Line 1 standard. This allows a calibration over the frequency range from 1.3GHz to 6GHz.

Fabricated Amplifier and TRL Calibration Kit



The amplifier and TRL calibration standards are fabricated on Arlon 25N 30mil thick PCB laminate.

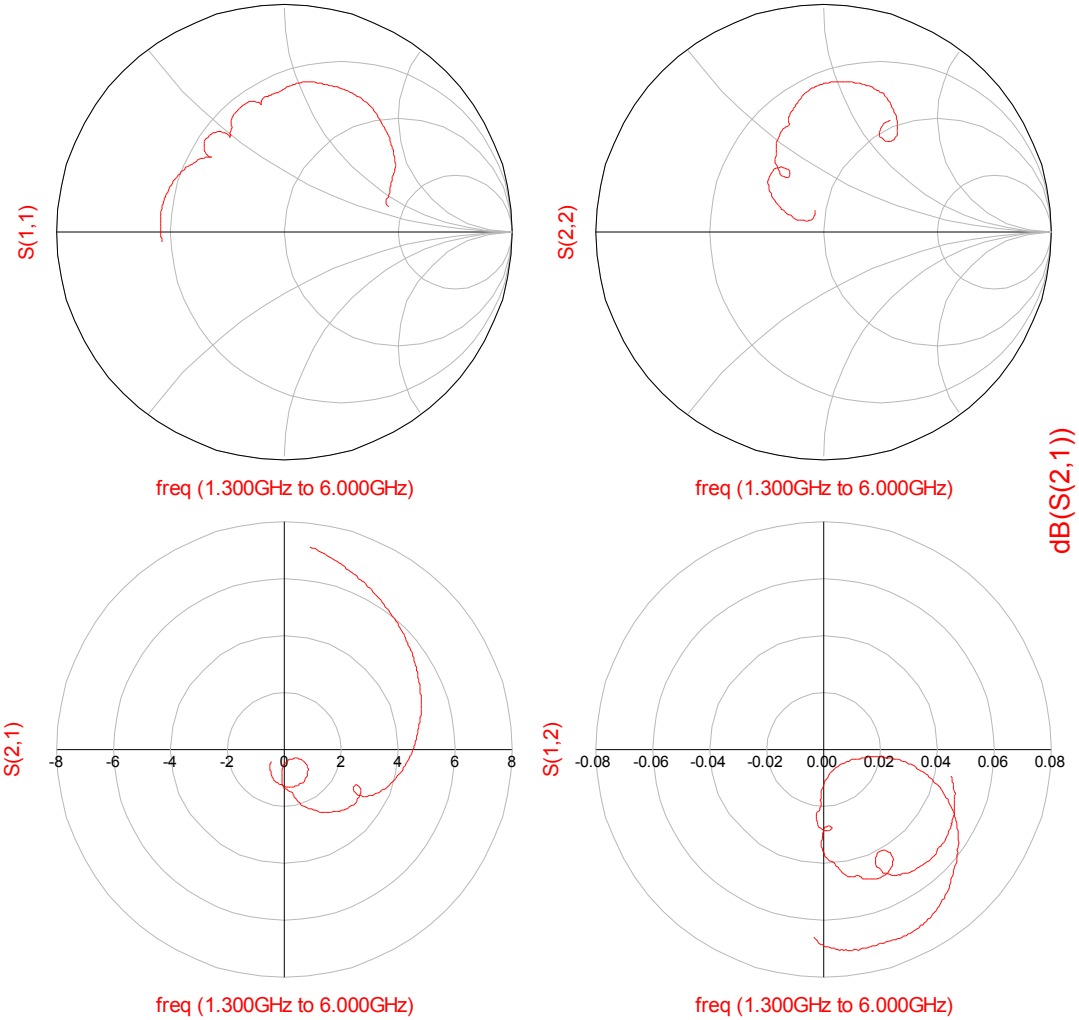
Amplifier S-Parameter Measurements Using TRL

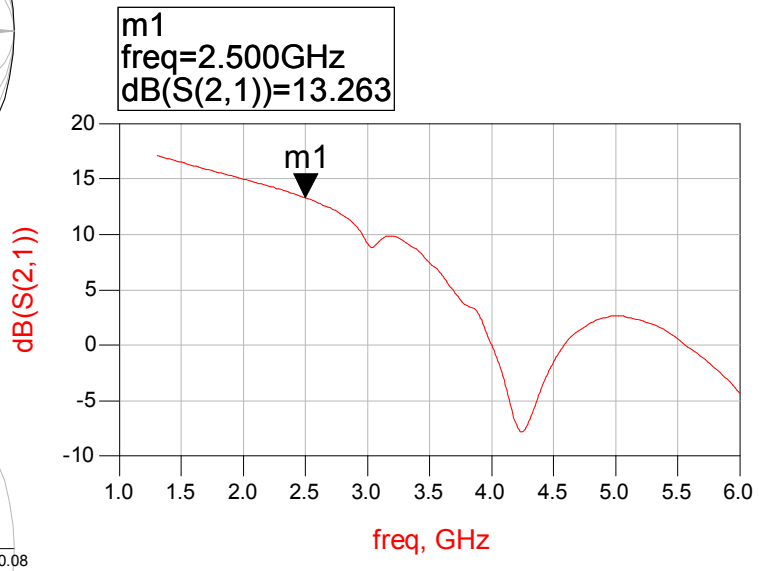


• The amplifier input matching network is not yet placed on the PCB. A DC blocking capacitor is used at the input instead of the 1.6pF matching capacitor in order to measure the amplifier s- parameters without the input matching network. This allows a stability measurement over a wider range of frequencies.

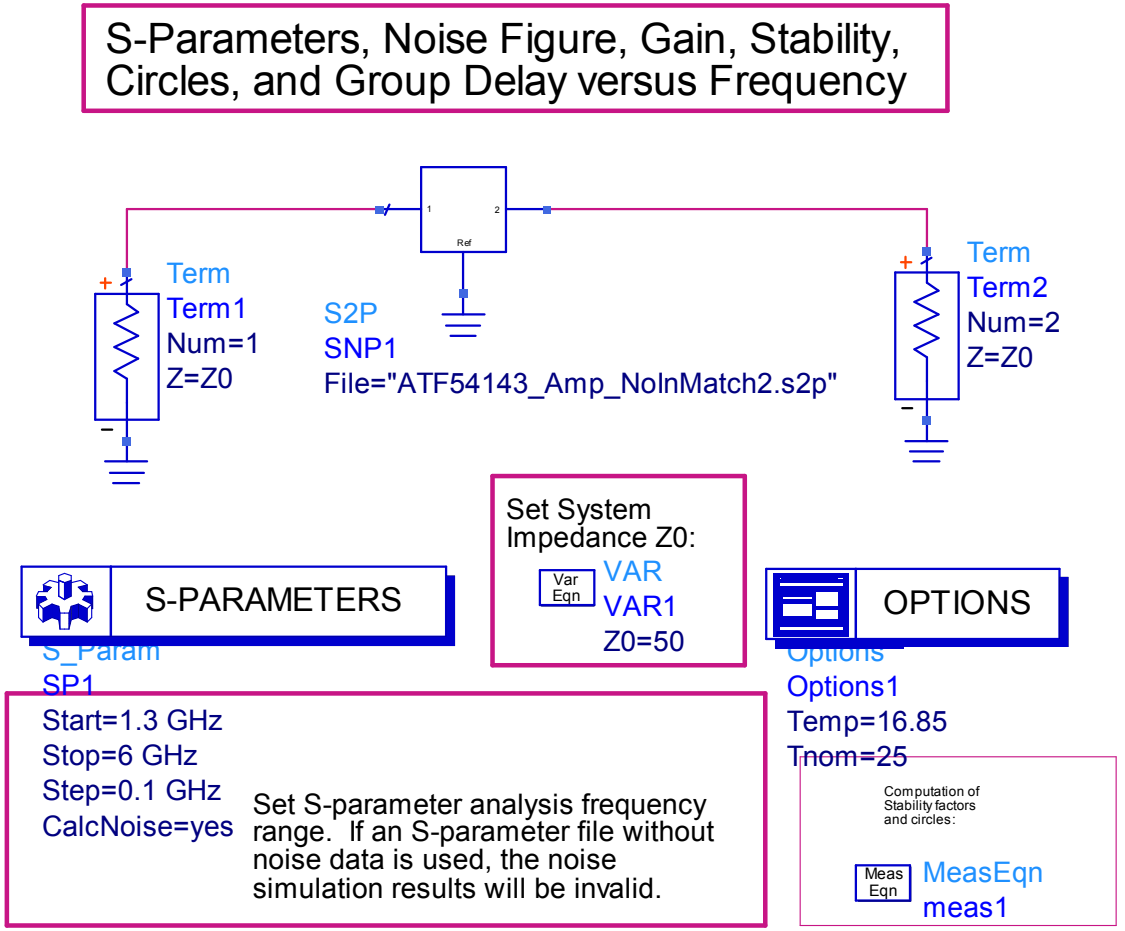
• Calibration coefficients are entered into the network analyzer. The network analyzer is calibrated using the Arlon 25N TRL calibration kit with the Line 1 standard. This allows a calibration from 1.3GHz to 6GHz.

Amplifier S-Parameter Measurements Using TRL



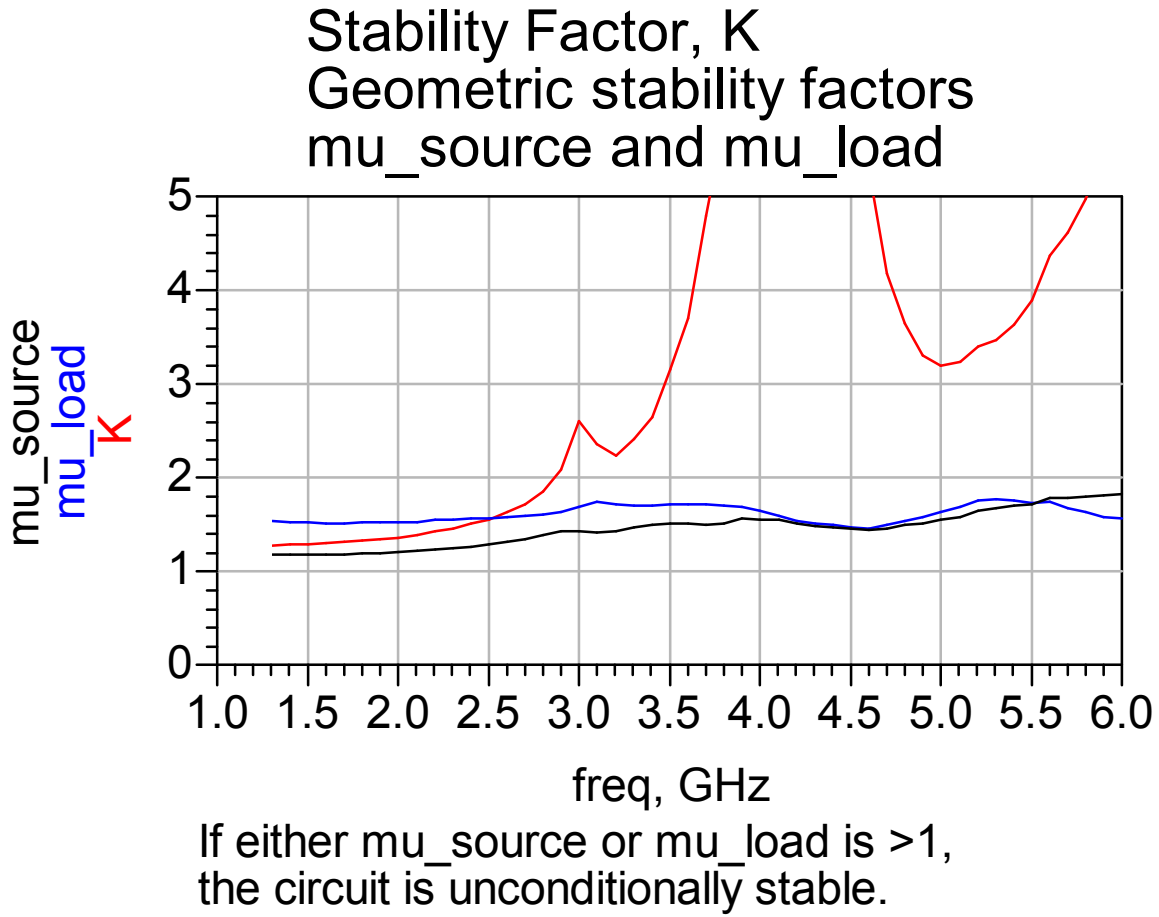


Measured Stability



The ADS design guide allows a stability analysis on the measured s-parameter data from 1.3GHz to 6GHz.

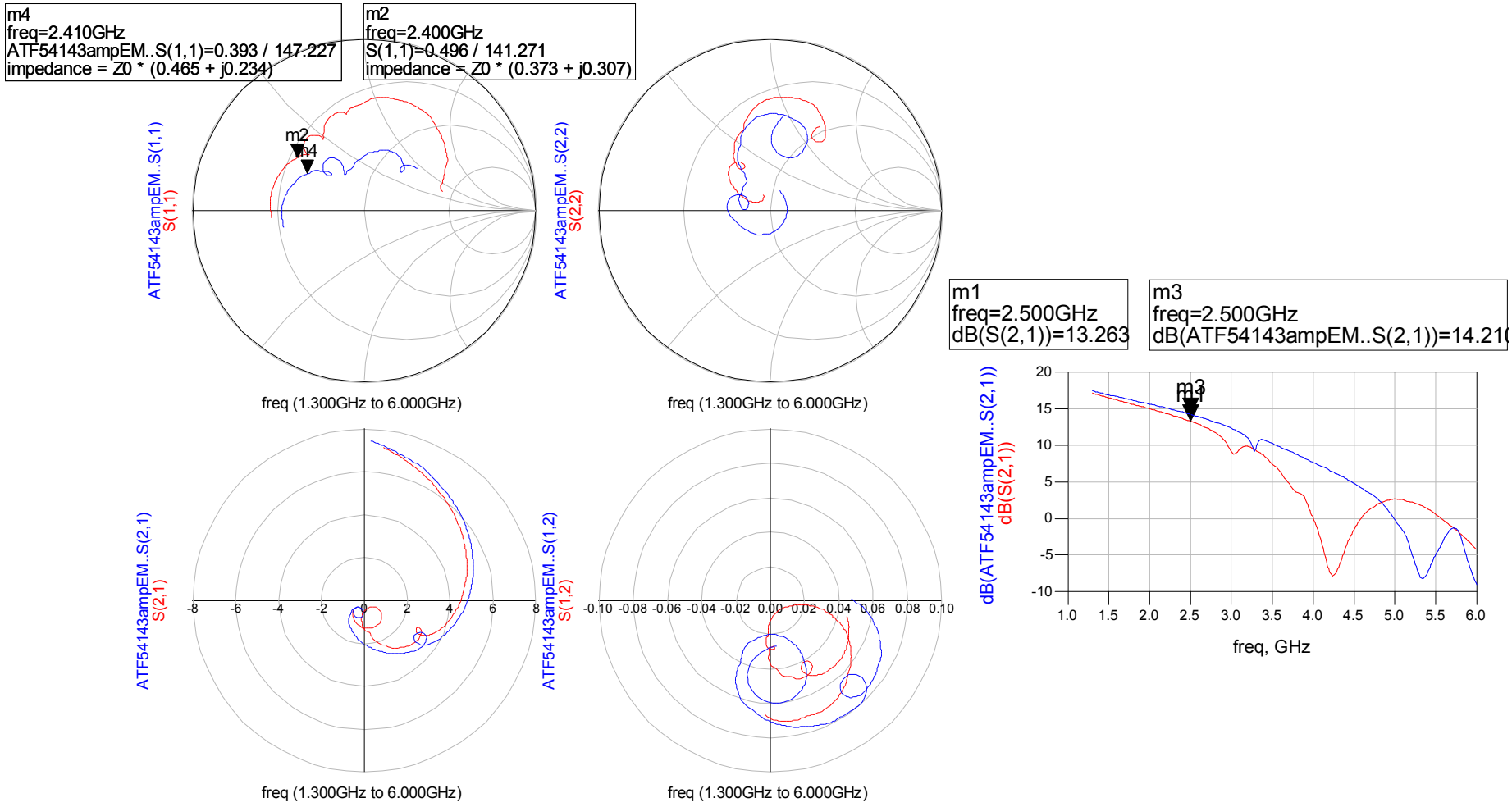
Measured Stability



If either mu_source or mu_load is >1,
the circuit is unconditionally stable.

• $\mu_{Source} \geq 1$ and $\mu_{Load} \geq 1$ for all frequencies from 1.3GHz to 6GHz, either of which, guarantee unconditional stability over that frequency range. Thus, the measured s-parameters indicate unconditional stability from 1.3GHz to 6GHz.

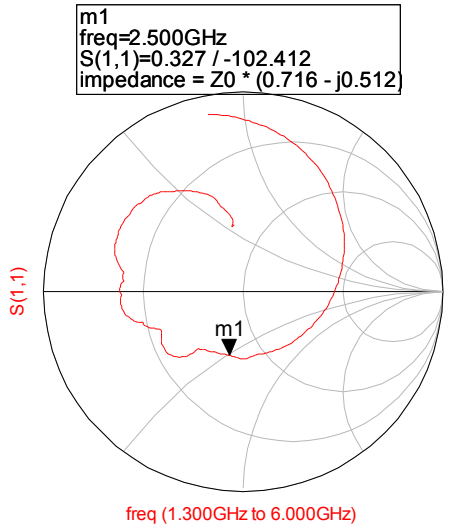
Measured Versus Modeled S-Parameters

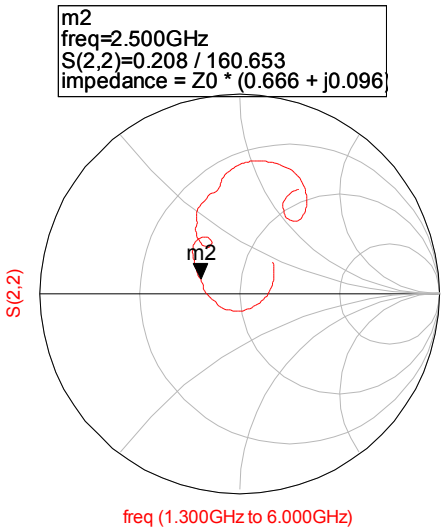


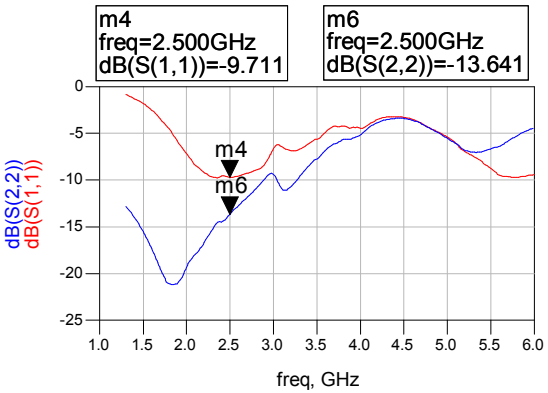
Measured Versus Modeled

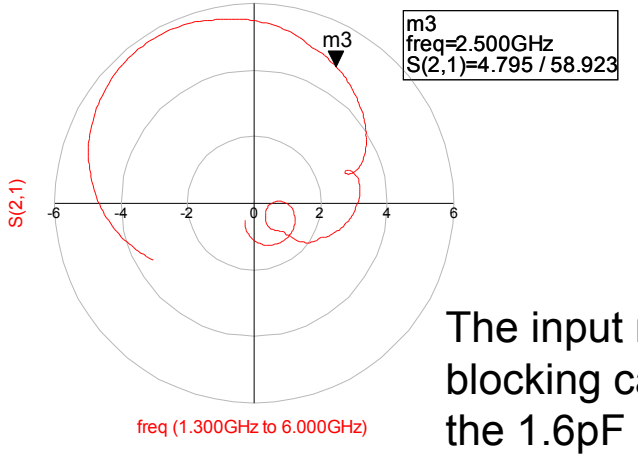
Good agreement is shown between the two results, particularly where the 27nH bias inductor is below it's self-resonant frequency. Measured gain at 2.5GHz is 13.26dB whereas the model predicts 14.2dB. Gain is very sensitive to source terminal ground inductance shown by previous analysis. Source terminal inductance was analyzed with EM simulation for both transistor source terminals. Then, these two inductances were combined in parallel to use in the circuit simulation. Some method of combining the two inductances is necessary since an s-parameter linear component in ADS has only one ground reference terminal. The input reflection coefficient at 2.5GHz is slightly higher for the measured amplifier versus the simulated amplifier. This accounts for a portion of the measured amplifier lower gain versus the simulated amplifier in the unmatched case. The method of combining parasitic transistor source terminal inductance and the higher input reflection coefficient of the measured amplifier easily leads to the gain discrepancy between modeled and measured results. Note that the measured amplifier exceeds the 12dB gain requirement.

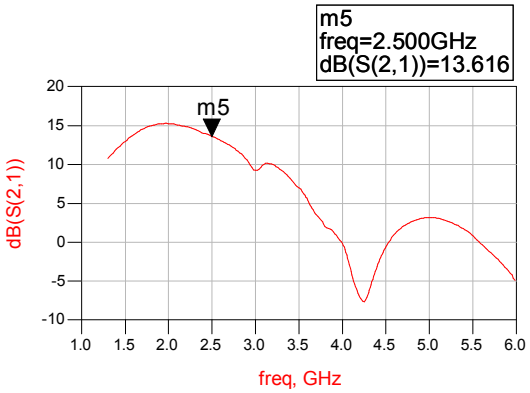
Complete Amplifier Measured S-Parameters









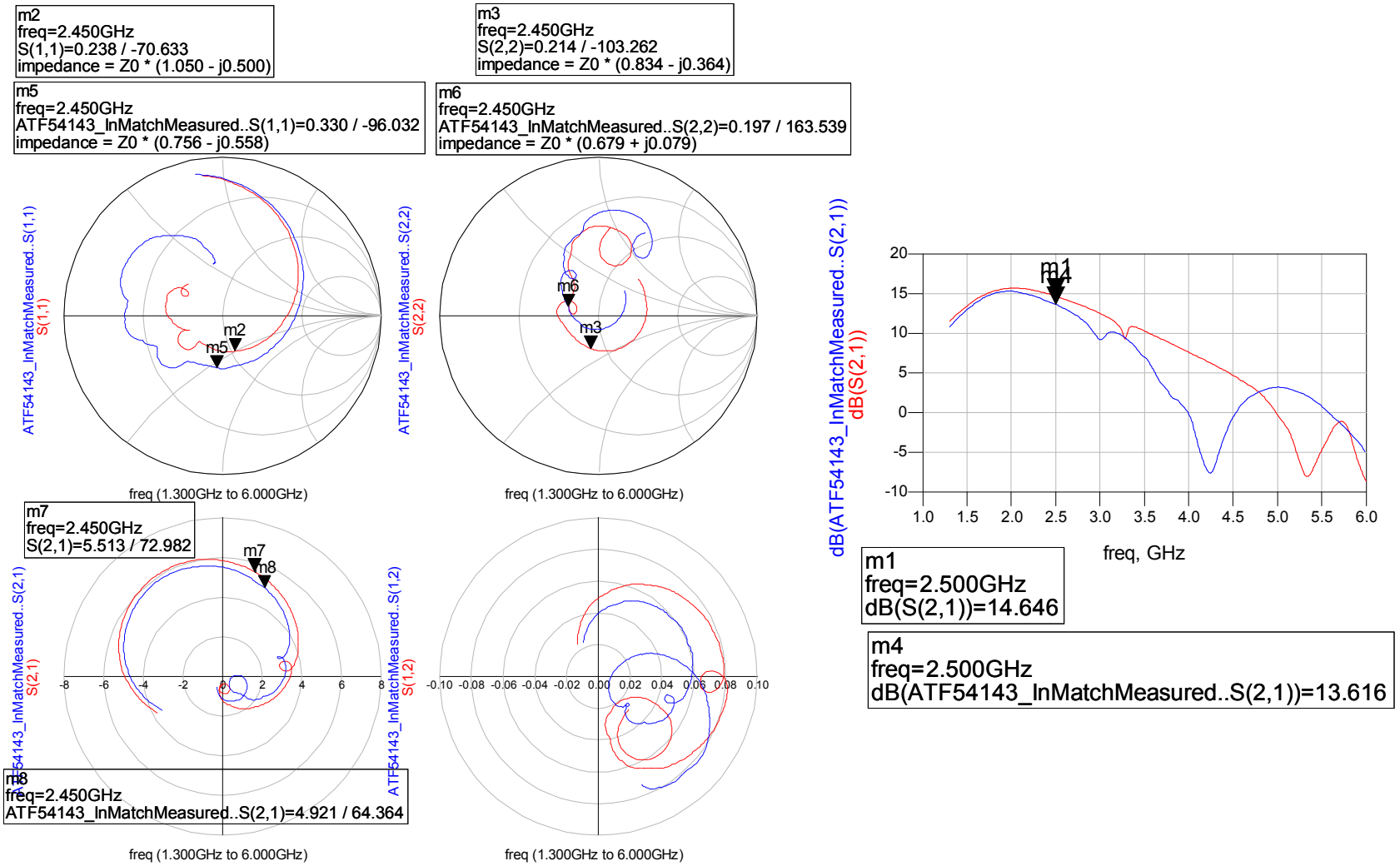


The input matching network is now added by removing the DC blocking capacitor C5 at the amplifier input and replacing it with the 1.6pF matching capacitor and adding the 2.4nH Coil Craft air wound inductor at location L3. The complete amplifier with the input matching network is re-measured and re-simulated.

Complete Amplifier Measured S-Parameters

The measured gain of 13.62dB is shown along with an input return loss of 9.7dB and an output return loss of 13.6dB. The measured gain is slightly below the simulated value (14.2dB) as was the case for the unmatched gain case because of the method used to estimate source ground parasitic inductance. The actual gain exceeds the 12dB specification requirement with margin, and is therefore acceptable. Note that the input return loss of 9.7dB marginally fails to the 10dB specification requirement, but will also be accepted in this particular design since the input return loss is considered to be a “soft” or negotiable specification. The output return loss of 13.64dB exceeds the 10dB goal with some margin.

Measured Versus Modeled



The plots show a close agreement between simulated and measured data.

Measured Versus Modeled

	Specification Requirement	Simulated Value	Measured Value
Frequency Range	2.4GHz to 2.48GHz	2.4GHz to 2.48GHz	2.4GHz to 2.48GHz
Gain	>12dB	14.65dB	13.62dB
Noise Figure	<2.5dB	1.78dB	1.91dB
IP3i	>0dBm	7dBm	13.7dBm
Input Return Loss	>10dB	12.7dB	9.7dB
Output Return Loss	>10dB	13.6dB	13.6dB
Current Drain	<100mA	61.38mA	63mA
Supply Voltage	3.3V	3.3V	3.3V
Stability	Unconditional	Unconditional	Unconditional

Conclusion

- Close agreement is obtained between the modeled and measured amplifier.
- A one-pass design was successful although design improvements may be possible. The goal was to design the circuit with the simulator, build the circuit, and have it meet all design goals without requiring PCB layout changes. This circuit met or exceeded all design goals.
- The gain of the actual amplifier was a bit lower than the model. This discrepancy is most likely due to the way the ground-return inductance was simulated.
- EM/Circuit Co-Simulation time is minimized since only the critical RF nodes are included in the EM portion of the analysis.
- Time and money are saved on the amplifier design process since multiple PCB passes are avoided by use of the simulation tools.

射 频 和 天 线 设 计 培 训 课 程 推 荐

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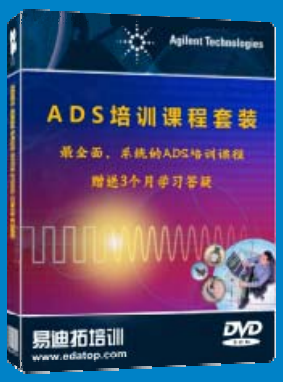

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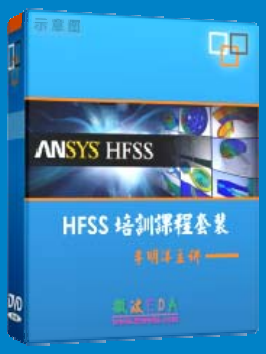

HFSS 学习培训课程套装

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